



**PRELIMINARY**

**W83759A**

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# **Advanced VL\_IDE Disk Controller**

## **W83759A PRODUCT SPECIFICATION**

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## GENERAL DESCRIPTION

The W83759A is an advanced version of Winbond's popular VL-IDE interface chip, the W83759. The W83759A retains all of the features and compatibility of the W83759 (the chip meets the ANSI ATA 4.0 specification for IDE hard disk operation and the VESA VL-Bus 2.0 specification for PC local bus devices) while incorporating new Enhanced IDE and Fast ATA features such as those described below.

**The enhanced ATA/IDE features that meet Enhanced IDE, SFF-8011, ATA-2, Fast-ATA specification:**

### Supports Disk Capacity of Greater than 528 MB

The W83759A's driver can handle remapping from BIOS CHS mode to HDD LBA mode. This scheme will enable users to break the 528 MB per drive barrier, allowing full use of BIOS INT13 CHS information in drives with a capacity of up to 8.4 GB.

### High Speed Host Transfer Rate

The W83759A supports Enhanced IDE PIO mode 3 and Fast ATA PIO mode 3 and 4 timing; jumper settings or driver programming can be used to select the PIO mode and a 33 or 50 MHz VL-Bus clock. Different programming timing can be selected for different drives in the same system. The burst transfer rate is shown in the following table.

ATA PIO mode	IDE Command Cycle Time (ns)	Burst Transfer Rate (MB/sec)	IORDY Throttle Control
0	600	3.33	Option
1	383	5.22	Option
2	240	8.33	Option
3	180	11.1	Required
4	120	16.6	Required

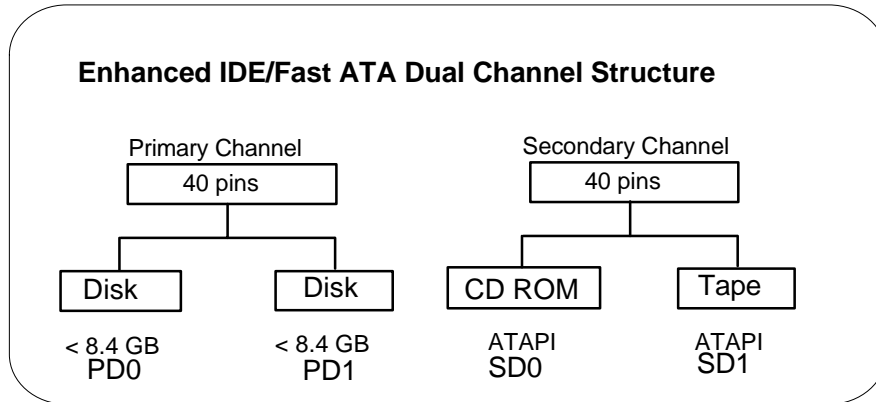
### Dual IDE Channels

Like the W83759, the W83759A supports a secondary IDE address (170h-177h/376h) and IRQ15 for applications with four hard disk drives. Additionally, the primary and secondary channels can be independently enabled or disabled by jumper settings or software programming.

### Non-disk IDE Peripherals

Because the command cycle can be programmed individually for each drive and dual IDE channels are supported, non-disk IDE peripherals (such as an ATAPI CD-ROM or tape drive) can be attached to the secondary IDE without affecting the transfer rate of the ATA disk drive. Sales of ATAPI IDE CD-

ROMs are expected to grow rapidly as these devices become a standard part of many users' desktop PC setup.



The W83759A puts all of the next generation ATA-IDE requirements together including support of high capacity disk drives; support of high speed host transfers; support of multiple IDE peripherals and support of non-disk IDE peripherals. It makes the high performance, low cost and "ease of use" IDE machine is possible.

The W83759A is pin-to-pin backward compatible with the W83759 chip. In addition to the advanced features described above, the W83759A supports automatic power-down, standby, and suspend APM power management states for green PC applications. This new chip is packaged in a 100-pin QFP.

Next table is the comparison of W83759 and W83759A:

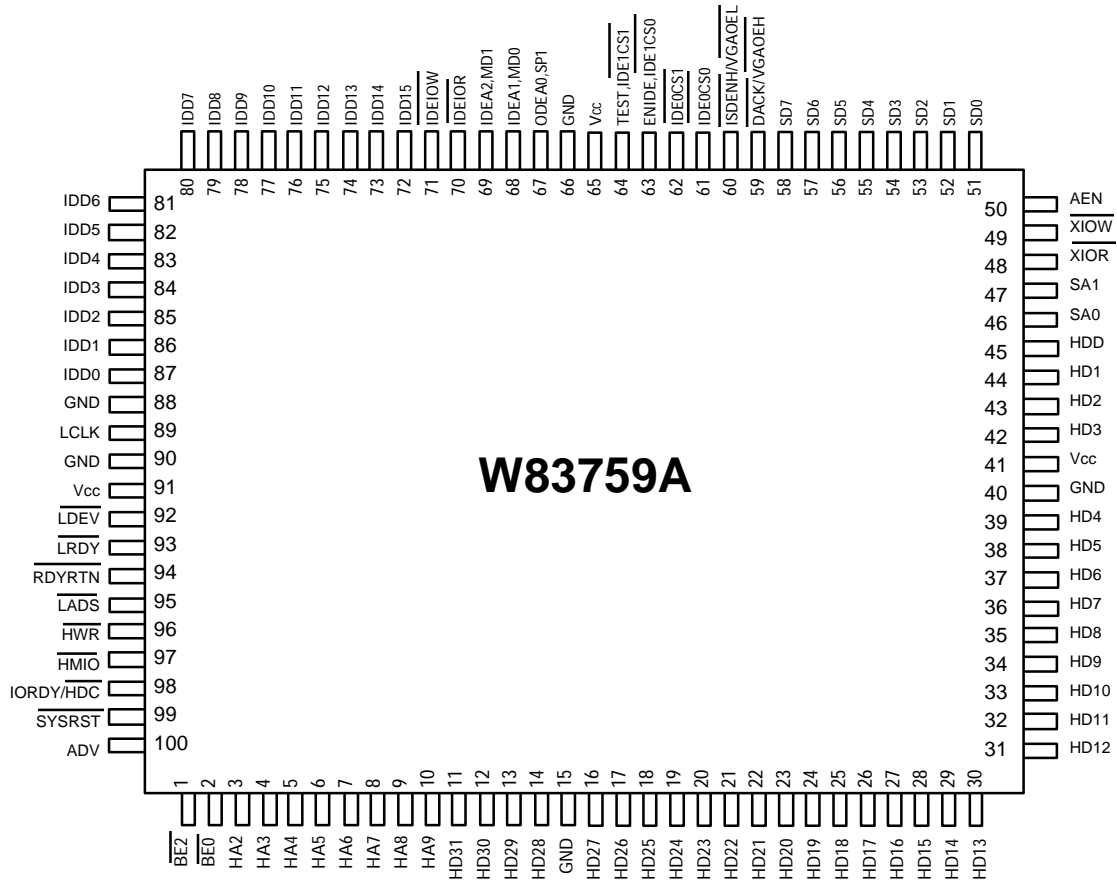
	W83759	W83759A
Dual Channel IDE	Yes	Yes
8.4 G Max. Cap.	software driving	software driving
PIO Mode 3,4 control	No	Yes*
DMA mode control	No	Yes*
IOCHRDY control	No	Yes*
IDE Timing control	jumper	jumper or driver*
Prefetch control	No	Yes*
Power saving control	No	Yes*
ATAPI protocol	software driving	software driving

\* All control are drive by drive (per drive selectability)

**FEATURE**

- Pin-to-pin backward compatible with W83759 VL\_IDE Interface chip.
- VESA VL\_Bus Rev 2.0 compatible , connects directly to local bus and four IDE drives.
- Direct interface to various ANSI ATA/ATA-2/FAST ATA/IDE-2/Enhanced IDE drives.
- Support 32 and 16-bit data transfer.
- Fully software programmable for command active/recovery time and address setup, data hold time.
- Built-in VL\_Bus to 16-bit IO data buffer for special application.
- Fully support Enhanced IDE feature include Fast PIO,Mode 3/4, IORDY flow control,Prefetch control.
- Support dual channel to allow up to four drives or non-disk device(ATAPI CD-ROM and tape drive).
- Pipeline pre-fetched reads and posted writes for concurrent disk and host operations.
- Independent access timing for all drives.(Primary/Secondary and Master/Slave)
- All Enhanced IDE new features may be disable/enable via driver or power on setting by Per Drive Select-ability.
- ATA/Mode 0-4 PIO speed may be set as default timing of each drive via power on jumper setting.
- Support slave DMA mode protocol.(Reserved)
- Support auto power down,standby,suspend APM power management state for Green-PC.
- Independently enable/disable primary and secondary channel by software or jumper setting.
- Support driver for DOS,Windows,OS/2,UNIX and Netware.
- 100 Pin QFP package.

PIN CONFIGURATION;@



W83759A

## PIN DESCRIPTION

SYMBOL	PIN	TYPE	DESCRIPTION
VL-Bus Interface			
ADV	100	I -PU	Advanced mode indicator. When high, the chip is in W83759A mode. When low, the chip is in W83759 mode.
LCLK	89	I	VL-Bus clock.
$\overline{\text{SYSRST}}$	99	I	System reset. When active, the power on setting pins act as input.
$\overline{\text{LADS}}$	95	I	Address data strobe. An active low input signal indicates that there is a valid address and command on the bus.
$\overline{\text{IORDY}}$ $\overline{\text{/HDC}}$	98	I	In W83759A mode: Enhanced IDE IORDY flow control input. Used to throttle disk's PIO data transfers to improve PIO mode. In W83759 mode: Host data or code status. Used to distinguish between IO and interrupt or halt cycles.
$\overline{\text{HMIO}}$	97	I -PU	Host memory or I/O status. Used to distinguish between memory and I/O cycles.
$\overline{\text{HWR}}$	96	I	Host write or read status. Used to distinguish between write and read cycles.
$\overline{\text{BE2}}$ $\overline{\text{BE0}}$	1 2	I	Byte enable bits 2 and 0 from the host CPU address bus. These active low inputs specify which bytes will be valid for host read and write data transfers. When $\overline{\text{BE2}}$ low, the host performs a 32-bit hard disk data transfer cycle while $\overline{\text{LDEV}}$ active.
$\overline{\text{LDEV}}$	92	O	Local device. An active low output signal which indicates that the current host CPU command cycle is a valid W83759A I/O address (1F0h or 170h).
$\overline{\text{LRDY}}$	93	Tri-O	Local ready. An active low output that indicates when a CPU transfer has been completed. During a cycle the $\overline{\text{LRDY}}$ will first be enabled and driven high. When the cycle is completed, $\overline{\text{LRDY}}$ will immediately be pulled low and will remain active for one T-state. Then it will drive high for one T-state before finally being disabled to end the sequence. This signal is shared with all other VL-Bus targets and driven by W83759A only during the time of the cycle that W83759A has claimed as its own.

$\overline{\text{RDYRTN}}$	94	I	Ready return. An active low signal that indicates the end of the current host CPU transfer. Usually RDYRTN is tied directly to the RDY signal of the host CPU.
HA[9:2]	10-3	I	Host address bits 9 through 2 from the host address bus.
HD[31:0]	11-14 19-39 42-45	I/O	Host data. This is the 32-bit bidirectional data bus that connects to the host CPU. HD[7:0] define the lowest data byte, while HD[31:24] define the most significant by the BE[2:0] signals. The HD bus is normally in a high impedance state and is driven by the W83759A only during data register (1F0h or 170h) read cycles and VGA (VGAOEH = 0 or VGAOEL = 0) read cycles.
Drive Interface			
$\overline{\text{PRDYEN}}$ $\overline{\text{/IDE0CS0}}$	61	I/O -PU	When $\overline{\text{SYSRST}}$ is active, this is an input that latches on the rising edge of $\overline{\text{SYSRST}}$ . PRDYEN -A high input enables the IORDY flow control function of the primary channel(IDE0) and a low input disables the IDE0's flow control function. $\overline{\text{IDE0CS0}}$ -When $\overline{\text{SYSRST}}$ is inactive,this pin is an active low output used to select the command block registers in the IDE0 drive (1F0h-1F7h).
$\overline{\text{SRDYEN}}$ $\overline{\text{/IDE0CS1}}$	62	I/O -PU	When $\overline{\text{SYSRST}}$ is active, this is an input that latches on the rising edge of $\overline{\text{SYSRST}}$ . SRDYEN -A high input enables the IORDY flow control function of the secondary channel(IDE1) and a low disables the IDE1's flow control function. $\overline{\text{IDE0CS1}}$ -When $\overline{\text{SYSRST}}$ is inactive,this pin is an active low output used to select the alternate status register of the control block registers in the IDE0 drive(3F6).
$\overline{\text{ENIDE}}$ $\overline{\text{/IDE1CS0}}$	63	I/O -PU	When $\overline{\text{SYSRST}}$ is active, this is an input that latches on the rising edge of $\overline{\text{SYSRST}}$ . ENIDE -In W83759 mode(ADV=low), this power-on-setting pin controls if the chip enable or disable. In W83759A mode (ADV= high), this pin controls if the IDE0 channel enable or disable. A high input enables and a low input disables the IDE0 channel. $\overline{\text{IDE1CS0}}$ -When $\overline{\text{SYSRST}}$ is inactive, this pin is an active low output and is used to select the command block registers in the IDE1 drive (170h-177h).

<p><math>\overline{\text{TEST}}</math> <math>/\text{IDE1CS1}</math></p>	<p>64</p>	<p>I/O -PU</p>	<p>When <math>\overline{\text{SYSRST}}</math> is active, this is an input that latches on the rising edge of <math>\overline{\text{SYSRST}}</math>.</p> <p><math>\overline{\text{TEST}}</math> -In W83759 mode, this power-on-setting pin controls if both dual channel enable or only primary channel enable. A high input enables IDE0 and IDE1 simultaneously and a low input enables DE0 only. In W83759A mode, this pin controls if the IDE1 channel enable or disable like as ENIDE controls the IDE0 channel.</p> <p><math>\overline{\text{IDE1CS1}}</math> -When <math>\overline{\text{SYSRST}}</math> is inactive, this pin is an active low output and is used to select the alternate status register of the control block registers in the IDE1 drive (376).</p>																				
<p><math>\overline{\text{EMD1}}</math> <math>/\text{IDEIOR}</math></p>	<p>70</p>	<p>I/O -PU</p>	<p>When <math>\overline{\text{SYSRST}}</math> is active, this is an input that latches on the rising edge of <math>\overline{\text{SYSRST}}</math></p> <p><math>\overline{\text{EMD1}}</math> -This power-on-setting pin combines with <math>\overline{\text{EMD0}}</math> to set the initial enhanced timing mode of hard disk access cycle when the enhanced mode is selected via the POSS3 configuration register.</p> <p><math>\overline{\text{IDEIOR}}</math> -Drive I/O read.</p> <p>An active low output that enables data to be read from the drive. The duration and repetition rate of <math>\overline{\text{IDEIOR}}</math> by the type of IDE drive, as specified by MD1 and MD0 in W83759 mode, or by <math>\overline{\text{EMD1}}</math> and <math>\overline{0}</math> in W83759A enhanced mode.</p>																				
<p><math>\overline{\text{EMD0}}</math> <math>/\text{IDEIOW}</math></p>	<p>71</p>	<p>I/O -PU</p>	<p>When <math>\overline{\text{SYSRST}}</math> is active, this is an input that latches on the rising edge of <math>\overline{\text{SYSRST}}</math></p> <p><math>\overline{\text{EMD0}}</math> -This power-on-setting pin combines with <math>\overline{\text{EMD1}}</math> to set the initial enhanced timing mode of hard disk access cycle when the enhanced mode is selected via the POSS3 configuration register.</p> <table border="1" data-bbox="690 1241 1274 1423"> <thead> <tr> <th>ATA PIO mode</th> <th>ACCESS TIME</th> <th><math>\overline{\text{EMD1}}</math></th> <th><math>\overline{\text{EMD0}}</math></th> </tr> </thead> <tbody> <tr> <td>2</td> <td>240nS</td> <td>1</td> <td>1</td> </tr> <tr> <td>3</td> <td>180nS</td> <td>1</td> <td>0</td> </tr> <tr> <td>3</td> <td>180nS</td> <td>0</td> <td>1</td> </tr> <tr> <td>4</td> <td>120nS</td> <td>0</td> <td>0</td> </tr> </tbody> </table> <p><math>\overline{\text{IDEIOW}}</math> -Drive I/O write.</p> <p>An active low output that enables data to be written to the drive. The duration and repetition rate of <math>\overline{\text{IDEIOW}}</math> cycles are determined by the type of IDE drive, as specified as <math>\overline{\text{IDEIOR}}</math>.</p>	ATA PIO mode	ACCESS TIME	$\overline{\text{EMD1}}$	$\overline{\text{EMD0}}$	2	240nS	1	1	3	180nS	1	0	3	180nS	0	1	4	120nS	0	0
ATA PIO mode	ACCESS TIME	$\overline{\text{EMD1}}$	$\overline{\text{EMD0}}$																				
2	240nS	1	1																				
3	180nS	1	0																				
3	180nS	0	1																				
4	120nS	0	0																				

<p>MD1 /IDEA2, MD0 /IDEA1</p>	<p>69  68</p>	<p>I/O -PD</p>	<p>When <u>SYSRST</u> is active, these pins function as inputs and latch on the rising edge of <u>SYSRST</u> . MD1,MD0 -ATA mode of IDE Drive. MD0 and MD1 are used to select the hard disk access time.</p> <table border="1" data-bbox="673 394 1242 577"> <thead> <tr> <th>ATA PIO mode</th> <th>ACCESS TIME</th> <th>MD1</th> <th>MD0</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>600nS</td> <td>0</td> <td>0</td> </tr> <tr> <td>0+</td> <td>500nS</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>400nS</td> <td>1</td> <td>0</td> </tr> <tr> <td>2</td> <td>240nS</td> <td>1</td> <td>1</td> </tr> </tbody> </table> <p>IDEA2,IDEA1 -IDE drive address bit2 and 1. Drive address bit2 and 1 are outputs to the IDE connector for register selection in the drive.</p>	ATA PIO mode	ACCESS TIME	MD1	MD0	0	600nS	0	0	0+	500nS	0	1	1	400nS	1	0	2	240nS	1	1
ATA PIO mode	ACCESS TIME	MD1	MD0																				
0	600nS	0	0																				
0+	500nS	0	1																				
1	400nS	1	0																				
2	240nS	1	1																				
<p>SP1 /IDEA0</p>	<p>67</p>	<p>I/O -PD</p>	<p>When <u>SYSRST</u> is active, this pin is an input that latches on the rising edge of <u>SYSRST</u> . SP1 -VL-Bus speed select. A high input configures the W83759A to run at over 33 MHz up to 50 MHz; a low input configures the W83759A to run at under 33MHz. IDEA0 -IDE drive address bit0. Drive address bit 0 is output to the IDE connector for register selection in the drive.</p>																				
<p>IDD[15:0]</p>	<p>72-87</p>	<p>I/O -PU</p>	<p>When <u>SYSRST</u> is active, these pins function as inputs and latch on the rising edge of <u>SYSRST</u> . As power on setting pin, IDD[15:8] are latched to the POSS3 register and IDD[7:0] are latched to the POSS2 register. As drive data bus. Bits 15 through 0 are the 16-bit bidirectional data bus that connects to the IDE drive. IDD[7:0] define the lowest data byte, while IDD bus is normally in a high impedance state and is driven by the W83759A only during IDE or VGA (VGAOEH = 0 or VGAOEL = 0) write cycles.</p>																				
<p>ISA-Bus Interface</p>																							
<p>SA[1:0]</p>	<p>47,46</p>	<p>I</p>	<p>ISA address bits 1 and 0. Used to select the hard disk I/O registers.</p>																				
<p>SD[7:0]</p>	<p>58-51</p>	<p>I/O</p>	<p>These signals provide data bus bits 0 through 7 for the CPU and IDE I/O devices. SD0 is the least significant bit and SD7 is the most significant bit.</p>																				

$\overline{\text{XIOR}}$	48	I	$\overline{\text{XIOR}}$ instructs the hard disk I/O device to drive its data onto the SD data bus.												
$\overline{\text{XIOW}}$	49	I	$\overline{\text{XIOW}}$ instructs the hard disk I/O device to read the data on the SD data bus.												
AEN	50	I	When this line is active (high), the DMA controller has control of the address bus. A low is the address enable.												
Special Bus Control Interface															
$\overline{\text{SUSP}}$ , $\overline{\text{DACK}}$ , $\overline{\text{VGAOEH}}$	59	I -PU	<p>This pin is a multi-function input pin.</p> <p><math>\overline{\text{SUSP}}</math> -In suspend enable mode, it indicates that the W83759A will enter the suspend state when low and resume when high.</p> <p><math>\overline{\text{DACK}}</math> -In DMA transfer enable mode, it is used to distinguish that when the DMA transfer cycle occurs.</p> <p><math>\overline{\text{VGAOEH}}</math> -In VGA buffer enable mode, this active low input controls the input enable for the data transceivers that connect the ID[15:0] pins to the HD[31:16] pins.</p>												
$\overline{\text{DMASL}}$ , $\overline{\text{VGAOEL}}$ $\overline{\text{ISDENH}}$	60	I/O -PU	<p>When <math>\overline{\text{SYSRST}}</math> is active, this pin is an input that latches on the rising edge of <math>\overline{\text{SYSRST}}</math>.</p> <p><math>\overline{\text{DMASL}}</math> -This power on setting pin combines with SUSPEN (IDD11 power on setting pin) to determine in which mode the W83759A is.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th><math>\overline{\text{DMASL}}</math></th> <th>SUSPEN</th> <th>Mode</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>X</td> <td>VGA buffer enable</td> </tr> <tr> <td>0</td> <td>1</td> <td>Suspend enable</td> </tr> <tr> <td>0</td> <td>0</td> <td>DMA transfer enable</td> </tr> </tbody> </table> <p><math>\overline{\text{VGAOEL}}</math> -In VGA buffer enable mode, this active low input controls the input enable for the data transceivers that connect the ID[15:0] pins to the HD[15:0] pins.</p> <p><math>\overline{\text{ISDENH}}</math> -In DMA transfer enable mode, this output pin controls the activity of high byte buffer between IDD[15:8] and SD{15:8}.</p>	$\overline{\text{DMASL}}$	SUSPEN	Mode	1	X	VGA buffer enable	0	1	Suspend enable	0	0	DMA transfer enable
$\overline{\text{DMASL}}$	SUSPEN	Mode													
1	X	VGA buffer enable													
0	1	Suspend enable													
0	0	DMA transfer enable													
Vcc	41,65, 91		+5V power supply												
GND	15,40, 66 88,90		Ground reference												

## CONFIGURATION REGISTERS

There are some configuration registers implemented in W83759A. These registers are always accessible in single-chip mode through the Index/Data port. The Index/Data port address is 1B4h/1B8h or 134h/138h depend on pin IDD0 is high or low at power-on setting. When in multi-chip mode (IDD1 is low at power-on setting), an ID code should be written to 1B0h/130h (IDIN port) then enter the programming sequence if the ID code matches the chip ID(determined by IDD2,IDD3 at power-on setting) or leave the programming sequence if not matches.After enter the programming sequence the chip ID can be read by reading 1BCh/13Ch (IDOUT port).

	IDD0_P is HIGH	IDD0_P is LOW
IDIN port (W/O)	1B0h*	130h**
Index port (R/W)	1B4h	134h
data port (R/W)	1B8h	138h
IDOUT port (R/O)	1BCh	13Ch

\* The alias base addresses of 1B0h are XB0h and YB0h,where the "X" means 0,4,8,C and "Y" means 1,5,9,D.

\*\* The alias base addresses of 130h are X30h and Y30h,where the "X" means 0,4,8,C and "Y" means 1,5,9,D.

**The Index map table of configuration registers:**

INDEX	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default Value
80h(R/O) POSS1	ADV	SP1	MD1	MD0	PRDYE N	SRDYE N	IDEN1	IDEN0	8Fh
81h(R/W) POSP1	ADV_P	SP1_P	MD1_P	MD0_P	PRDYE N_P	SRDYE N_P	IDEN1_ P	IDEN0_ P	8Fh
82h(R/O) POSS2	PD0LEN	PD1LEN	SD0LEN	SD1LEN	DSL1	DSL0	CRLK#	CRSL	FFh
83h(R/W) POSP2	PD0LE_ P	PD1LEN_ P	SD0LEN_ P	SD1LEN_ P	DSL1_P	DSL0_P	CRLK#_ P	CRSL_P	FFh
84h(R/O) POSS3	PD0EM#	PD1EM#	SD0EM#	SD1EM#	SUSPE N	STBY#	APD	SWAP#	FFh
85h(R/W) POSP3	PD0EM# _P	PD1EM# _P	SD0EM# _P	SD1EM# _P	SUSPE N_P	STBY#_ P	APD_P	SWAP# _P	FFh
86h(R/W) ALTCTL	DMASL# _P	Reserved	EMD1	EMD0	PEMD1_ P	PEMD0_ P	SEMD1_ P	SEMD0_ P	80h
87h(R/O) REVID	DMASL#	Reserved	PDRV	SDRV	Rev 3	Rev 2	Rev 1	Rev 0	8Ah
88h(R/W) PD0TIM0	PD0ACT 3	PD0ACT 2	PD0ACT 1	PD0ACT 0	PD0RC V3	PD0RC V2	PD0RC V1	PD0RCV 0	00h
89h(R/W) PD0TIM1	PD0AST 1	PD0AST 0	PD0DHT 1	PD0DHT 0	PD0PRE #	PD0DM A#	PD0RD Y#	PD0ADV	00h
8Ah(R/W) PD1TIM0	PD1ACT 3	PD1ACT 2	PD1ACT 1	PD1ACT 0	PD1RC V3	PD1RC V2	PD1RC V1	PD1RCV 0	00h
8Bh(R/W) PD1TIM1	PD1AST 1	PD1AST 0	PD1DHT 1	PD1DHT 0	PD1PRE #	PD1DM A#	PD1RD Y#	PD1ADV	00h
8Ch(R/W) SD0TIM0	SD0ACT 3	SD0ACT 2	SD0ACT 1	SD0ACT 0	SD0RC V3	SD0RC V2	SD0RC V1	SD0RCV 0	00h
8Dh(R/W) SD0TIM1	SD0AST 1	SD0AST 0	SD0DHT 1	SD0DHT 0	SD0PRE #	SD0DM A#	SD0RD Y#	SD0ADV	00h
8Eh(R/W) SD1TIM0	SD1ACT 3	SD1ACT 2	SD1ACT 1	SD1ACT 0	SD1RC V3	SD1RC V2	SD1RC V1	SD1RCV 0	00h
8Fh(R/W) SD1TIM1	SD1AST 1	SD1AST 0	SD1DHT 1	SD1DHT 0	SD1PRE #	SD1DM A#	SD1RD Y#	SD1ADV	00h

CRX80h (POSS1)

Read Only

Power On Setting Status 1

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADV	SP1	MD1	MD0	PRDYEN	SRDYEN	IDEN1	IDEN0

Bit 7	ADV	Power on setting value of ADV pin Initial application mode	
	0	None advanced mode application	
	<u>1</u>	<u>Advanced mode application</u>	
Bit 6	SP1	Power on setting value of IDEA0 pin Select VESA bus operating CLK	
	0	<u>VLCLK 33 MHz</u>	
	<u>1</u>	VLCLK > 33 MHz	
Bit 5,4	MD1,MD0	Power on setting value of IDEA2 , IDEA1 pin Default HDD host transfer mode	
		MD1 MD0	
		<u>0</u> <u>0</u>	Mode 0 (cycle time = 600 ns)
		0 1	Mode 0+ (cycle time = 500 ns)
		1 0	Mode 1 (cycle time = 400 ns)
		1 1	Mode 2 (cycle time = 240 ns)
Bit 3	PRDYEN	Power on setting value of IDE0CS0 pin Initial state of Primary channel IOCHRDY flow control	
		0	Disable IOCHRDY flow control
		<u>1</u>	<u>Enable IOCHRDY flow control</u>
Bit 2	SRDYEN	Power on setting value of IDE0CS1 pin Initial state of Secondary channel IOCHRDY flow control	
		0	Disable IOCHRDY flow control
		<u>1</u>	<u>Enable IOCHRDY flow control</u>
Bit 1,0	IDEN1,IDEN0	Power on setting value of IDE1CS1,IDE1CS0 pin Initial state of IDE ENable control	
	when ADV_P =0	IDEN1	IDEN0
		X	0
		0	1
		<u>1</u>	<u>1</u>
			Primary IDE
			Secondary IDE
			disable
			disable
			<u>enable</u>
			<u>enable</u>

when ADV_P =1	IDEN1	IDEN0	Primary IDE	Secondary IDE
	0	0	disable	disable
	1	0	disable	enable
	0	1	enable	disable
	<u>1</u>	<u>1</u>	<u>enable</u>	<u>enable</u>

CRX81h (POSP1)                      Read / Write                      Power On Setting Programming 1

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADV_P	SP1_P	MD1_P	MD0_P	PRDYEN_P	SRDYEN_P	IDEN1_P	IDEN0_P

After power on, the content of POSP1 register is equal to POSS1 register. The host can program the POSP1 and alternate the effect of power on setting .

Bit 7	ADV_P	Programming application mode
		0            None advanced mode application
		<u>1</u> <u>Advanced mode application</u>
Bit 6	SP1_P	Select VESA bus operating CLK
		<u>0</u> <u>VLCLK 33 MHz</u>
		1            VLCLK > 33 MHz
Bit 5,4	MD1_P, MD0_P	Select default HDD host transfer mode
		MD1_P    MD0_P
		<u>0</u> <u>0</u> <u>Mode 0 (cycle time = 600 ns)</u>
		0        1        Mode 0+ (cycle time = 500 ns)
		1        0        Mode 1 (cycle time = 400 ns)
		1        1        Mode 2 (cycle time = 240 ns)
Bit 3	PRDYEN_P	Primary channel IOCHRDY flow control
		0            Disable IOCHRDY flow control
		<u>1</u> <u>Enable IOCHRDY flow control</u>
Bit 2	SRDYEN_P	Secondary channel IOCHRDY flow control
		0            Disable IOCHRDY flow control
		<u>1</u> <u>Enable IOCHRDY flow control</u>
Bit 1,0	IDEN1_P, IDEN0_P	IDE ENable control

when ADV_P =0	IDEN1_P	IDEN0_P	Primary IDE	Secondary IDE
	x	0	disable	disable
	0	1	enable	disable
	<u>1</u>	<u>1</u>	<u>enable</u>	<u>enable</u>

when ADV_P =1	IDEN1_P	IDEN0_P	Primary IDE	Secondary IDE
	0	0	disable	disable
	1	0	disable	enable
	0	1	enable	disable
	<u>1</u>	<u>1</u>	<u>enable</u>	<u>enable</u>

CRX82h (POSS2)                      Read Only                      Power On Setting Status 2

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PD0LEN	PD1LEN	SD0LEN	SD1LEN	DSL1	DSL0	CRLK#	CRSL

Bit 7      PD0LEN    Power on setting value of IDD7 pin  
Initial Primary Drive0 (PD0) local device control

0            Disable local device  
1            Enable local device

Bit 6      PD1LEN    Power on setting value of IDD6 pin  
Initial Primary Drive1 (PD1) local device control

0            Disable local device  
1            Enable local device

Bit 5      SD0LEN    Power on setting value of IDD5 pin  
Initial SecondaryDrive0 (SD0) local device control

0            Disable local device  
1            Enable local device

Bit 4      SD1LEN    Power on setting value of IDD4 pin  
Initial Secondary Drive1(SD1) local device control

0            Disable local device  
1            Enable local device

Bit 3,2      DSL1,0    Power on setting value of IDD3,IDD2 pin  
Initial Device ID selection (Using when in Multi-chip mode or

CR protection scheme)

DSL1	DSL0	Device ID
0	0	60h
0	1	61h
1	0	62h
<u>1</u>	<u>1</u>	<u>63h</u>

Bit 1	CRLK#	Power on setting value of IDD1 pin Initial Configuration Register locked control
		0 CR is auto-locked (using when Multi-chip mode)
		<u>1</u> <u>CR is not auto-locked (using when Single-chip mode)</u>
Bit 0	CRSL	Power on setting value of IDD0 pin Initial Configuration Register selection
		0 CR port address: 130h,134h,138h,13Ch
		<u>1</u> <u>CR port address: 1B0h,1B4h,1B8h,1BCh</u>

CRX83h (POSP2)                      Read / Write                      Power On Setting Programming 2

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PD0LEN_P	PD1LEN_P	SD0LEN_P	SD1LEN_P	DSL1_P	DSL0_P	CRLK#_P	CRSL_P

After power on, the content of POSP2 register is equal to POSS2 register. The host can program the POSP2 and alternate the effect of power on setting .

Bit 7	PD0LEN_P	Primary Drive0 (PD0) local device control
		0 Disable local device
		<u>1</u> <u>Enable local device</u>
Bit 6	PD1LEN_P	Primary Drive1 (PD1) local device control
		0 Disable local device
		<u>1</u> <u>Enable local device</u>
Bit 5	SD0LEN_P	Secondary Drive0 (SD0) local device control
		0 Disable local device
		<u>1</u> <u>Enable local device</u>
Bit 4	SD1LEN_P	Secondary Drive1(SD1) local device control
		0 Disable local device

1      Enable local device

Bit 3,2      DSL1,0\_P      Device ID selection (Using when in Multi-chip mode or CR protection scheme)

DSL1_P	DSL0_P	Device ID
0	0	60h
0	1	61h
1	0	62h
<u>1</u>	<u>1</u>	<u>63h</u>

Bit 1 CRLK#\_P      Configuration Register locked control

0      CR is auto-locked (using when Multi-chip mode)  
1      CR is not auto-locked (using when Single-chip mode)

Bit 0      CRSL\_P      Configuration Register selection

0      CR port address: 130h,134h,138h,13Ch  
1      CR port address: 1B0h,1B4h,1B8h,1BCh

CRX84h (POSS3)      Read Only      Power On Setting Status 3

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PD0EM#	PD1EM#	SD0EM#	SD1EM#	SUSPEN	STBY#	APD	SWAP#

Bit 7      PD0EM#      Power on setting value of IDD15 pin  
 Initially setting of PD0 enhanced timing enable

0      Enhanced timing  
1      Programmable timing

Bit 6      PD1EM#      Power on setting value of IDD14 pin  
 Initially setting of PD1 enhanced timing enable

0      Enhanced timing  
1      Programmable timing

Bit 5      SD0EM#      Power on setting value of IDD13 pin  
 Initially setting of SD0 enhanced timing enable

0      Enhanced timing  
1      Programmable timing

Bit 4      SD1EM#      Power on setting value of IDD12 pin  
 Initially setting of SD1 enhanced timing enable

0      Enhanced timing

		<u>1</u>	<u>Programmable timing</u>
Bit 3	SUSPEN	Power on setting value of IDD11 pin Initially setting of SUSPend function	
		0	Support DMA mode if DMASL#_P=0 and ADV_P=1
		<u>1</u>	Support suspend function if DMASL#_P=0 and ADV_P=1.
Bit 2	STBY#	Power on setting value of IDD10 pin Initially setting of STandBy state	
		0	W83759A is in standby state
		<u>1</u>	<u>W83759A is in normal state</u>
Bit 1	APD	Power on setting value of IDD9 pin Initially setting of Auto Power Down	
		0	Auto Power Down off
		<u>1</u>	<u>Auto Power Down on</u>
Bit 0	SWAP#	Power on setting value of IDD8 pin Initially Primary,Secondary channel connection select	
		0	Primary channel connect to IDE1 Secondary channel connect to IDE0
		<u>1</u>	<u>Primary channel connect to IDE0</u> <u>Secondary channel connect to IDE1</u>

CRX85h (POSP3)                      Read/ Write                      Power On Setting Programming 3

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PD0EM#_P	PD1EM#_P	SD0EM#_P	SD1EM#_P	SUSPEN_P	STBY#_P	APD_P	SWAP#_P

Bit 7	PD0EM#_P	Power on setting programming of IDD15 pin Programmable setting of PD0 ehanced timing enable	
		0	Enhanced timming
		<u>1</u>	<u>Programmable timing</u>
Bit 6	PD1EM#_P	Power on setting programming of IDD14 pin Programmable setting of PD1 ehanced timing enable	
		0	Enhanced timming
		<u>1</u>	<u>Programmable timing</u>
Bit 5	SD0EM#_P	Power on setting programming of IDD13 pin Programmable setting of SD0 ehanced timing enable	

		0	Enhanced timing
		<u>1</u>	<u>Programmable timing</u>
Bit 4	SD1EM#_P		Power on setting programming of IDD12 pin Programmable setting of SD1 enhanced timing enable
		0	Enhanced timing
		<u>1</u>	<u>Programmable timing</u>
Bit 3	SUSPEN_P		Power on setting value of IDD11 pin Programmable setting of SUSPend function
		0	Support suspend function if DMASL#_P=0 and ADV_P=1
		<u>1</u>	<u>Support DMA transfer if DMASL#_P=0 and ADV_P=1</u>
Bit 2	STBY#_P		Power on setting value of IDD10 pin Programmable setting of STandBy state
		0	W83759A is in standby state
		<u>1</u>	<u>W83759A is in normal state</u>
Bit 1	APD_P		Power on setting value of IDD9 pin Initially setting of Auto Power Down
		0	Auto Power Down off
		<u>1</u>	<u>Auto Power Down on</u>
Bit 0	SWAP#_P		Power on setting programming of IDD8 pin Programmable Primary,Secondary channel connection select
		0	Primary channel connect to IDE1 Secondary channel connect to IDE0
		<u>1</u>	<u>Primary channel connect to IDE0 Secondary channel connect to IDE1</u>

CRX86h (ALTCTL)

Read / Write

Alternative Control Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DMASL#_P	Reserved	EMD1	EMD0	PEMD1_P	PEMD0_P	SEMD1_P	SEMD0_P

Bit 7	DMASL#_P		Power on setting value of $\overline{\text{VGAOEL}}$ pin. After power on, this bit can be programmed to alternate the effect of DMA disable/enable power on setting.
		0	DMA mode enable if SUSPEN_P=0 and ADV_P=1

1      DMA mode disable

Bit 6      Reserved      0 (default)

Bit5-4      EMD1,0 (Read Only)      Inverse of power-on setting value of IDEIOR ,IDEIOW pin  
Initially setting of Enhanced timing of IDE0 and IDE1.

EMD1	EMD0	ATA PIO Mode	Cycle time (ns)
<u>0</u>	<u>0</u>	<u>2</u>	<u>240</u>
0	1	3	180
1	0	3	180
1	1	4	120

Bit3-2      PEMD1,0\_P      Initially setting of Primary drive Enhanced timing  
After power on, these bits can be programmed to alternate the primary drive Enhanced timing.

PEMD1_P	PEMD0_P	ATA PIO mode	Cycle time (ns)
<u>0</u>	<u>0</u>	<u>2</u>	<u>240</u>
0	1	3	180
1	0	3	180
1	1	4	120

Bit1-0      SEMD1,0\_P      Initially setting of Secondary drive Enhanced timing  
After power on, these bits can be programmed to alternate the secondary drive Enhanced timing

SEMD1_P	SEMD0_P	ATA PIO Mode	Cycle time (ns)
<u>0</u>	<u>0</u>	<u>2</u>	<u>240</u>
0	1	3	180
1	0	3	180
1	1	4	120

CRX87h (REVID)      Read Only      Revision ID Number

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DMASL#	Reserved	PDRV	SDRV	Rev 3	Rev 2	Rev 1	Rev 0

Bit 7      DMASL#      Power on setting value of VGAOEL pin.  
The initially DMA enable/disable setting

0      DMA mode enable if SUSPEN\_P=0 and ADV\_P=1  
1      DMA mode disable

- Bit 6      Reserved      0 (default)  
            (Read/Write)
  
- Bit 5      PDRV            Primary channel current drive select
  - 0      Master drive (default)
  - 1      Slave drive
  
- Bit 4      SDRV            Secondary channel current drive select
  - 0      Master drive (default)
  - 1      Slave drive
  
- Bit 3-Bit 0 Rev 3-Rev 0    1010b (default when A version)

CRX88h (PD0TIM0)      Read/Write      Primary Drive0 Timing Control 0

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PD0ACT3	PD0ACT2	PD0ACT1	PD0ACT0	PD0RCV3	PD0RCV2	PD0RCV1	PD0RCV0

Bit 7-Bit 4 PD0ACT3~0    PD0 Data Register Port (1F0h) Read/Write Active Time

Read/Write active time (clocks)

<u>0000</u>	<u>17/16</u>
0001	3/2
0010	3/2
0011	4/3
0100	5/4
0101	6/5
0110	7/6
0111	8/7
1000	9/8
1001	10/9
1010	11/10
1011	12/11
1100	13/12
1101	14/13
1110	15/14
1111	16/15

Bit 3-Bit 0 PD0RCV3~0    PD0 Data Register Port (1F0h) Read/Write Recovery Time

Write/Read recovery time (clocks)

<u>0000</u>	<u>16/15</u>
0001	2/1
0010	2/1
0011	3/2
0100	4/3
0101	5/4
0110	6/5
0111	7/6
1000	8/7
1001	9/8
1010	10/9
1011	11/10
1100	12/11
1101	13/12
1110	14/13
1111	15/14

CRX89h (PD0TIM1)      Read/Write      Primary Drive0 Timing Control 1

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PD0AST1	PD0AST0	PD0DHT1	PD0DHT0	PD0PRE#	PD0DMA#	PD0RDY#	PD0ADV

Bit 7-Bit 6 PD0AST1~0      PD0 Data Register Port (1F0h) Address Setup Time

Read/Write extra address setup time (clocks)

<u>00</u>	<u>0</u>
01	2
10	2
11	3

Bit 5-Bit 4 PD0DHT1~0      PD0 Data Register Port (1F0h) Data Hold Time

Read/Write extra data hold time (clocks)

<u>00</u>	<u>0</u>
01	2
10	2
11	3

Bit 3 PD0PRE#	Prefetch/Post write control				
	<table border="0"> <tr> <td style="text-align: center;"><u>0</u></td> <td><u>Prefetch/Post write Enable</u></td> </tr> <tr> <td style="text-align: center;">1</td> <td><u>Prefetch/Post write Disable</u></td> </tr> </table>	<u>0</u>	<u>Prefetch/Post write Enable</u>	1	<u>Prefetch/Post write Disable</u>
<u>0</u>	<u>Prefetch/Post write Enable</u>				
1	<u>Prefetch/Post write Disable</u>				
Bit 2 PD0DMA#	PD0 DMA mode control				
	<table border="0"> <tr> <td style="text-align: center;"><u>0</u></td> <td><u>DMA mode Enable</u></td> </tr> <tr> <td style="text-align: center;">1</td> <td><u>DMA mode Disable</u></td> </tr> </table>	<u>0</u>	<u>DMA mode Enable</u>	1	<u>DMA mode Disable</u>
<u>0</u>	<u>DMA mode Enable</u>				
1	<u>DMA mode Disable</u>				
Bit 1 PD0RDY#	PD0 Data Register Port (1F0h) IOCHRDY Control				
	<table border="0"> <tr> <td style="text-align: center;"><u>0</u></td> <td><u>IOCHRDY Enable</u></td> </tr> <tr> <td style="text-align: center;">1</td> <td><u>IOCHRDY Disable</u></td> </tr> </table>	<u>0</u>	<u>IOCHRDY Enable</u>	1	<u>IOCHRDY Disable</u>
<u>0</u>	<u>IOCHRDY Enable</u>				
1	<u>IOCHRDY Disable</u>				
Bit 0 PD0ADV	PD0 Data Register Port (1F0h) Advanced Timing Enable				
	<table border="0"> <tr> <td style="text-align: center;"><u>0</u></td> <td><u>Normal timing</u> <u>(depend on SP1,MD1,MD0 setting)</u></td> </tr> <tr> <td style="text-align: center;">1</td> <td><u>Advanced timing</u> <u>(depend on PD0TIM1~0 setting)</u></td> </tr> </table>	<u>0</u>	<u>Normal timing</u> <u>(depend on SP1,MD1,MD0 setting)</u>	1	<u>Advanced timing</u> <u>(depend on PD0TIM1~0 setting)</u>
<u>0</u>	<u>Normal timing</u> <u>(depend on SP1,MD1,MD0 setting)</u>				
1	<u>Advanced timing</u> <u>(depend on PD0TIM1~0 setting)</u>				

CRX8Ah (PD1TIM0)      Read/Write      Primary Drive1 Timing Control 0

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PD1ACT3	PD1ACT2	PD1ACT1	PD1ACT0	PD1RCV3	PD1RCV2	PD1RCV1	PD1RCV0

Bit 7-Bit 4 PD1ACT3~0      PD1 Data Register Port (1F0h) Read/Write Active Time

Definition of these bits same as PD0ACT3~0

Bit 3-Bit 0 PD1RCV3~0      PD1 Data Register Port (1F0h) Read/Write Recovery Time

Definition of these bits same as PD0RCV3~0

CRX8Bh (PD1TIM1)      Read/Write      Primary Drive1 Timing Control 1

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PD1AST1	PD1AST0	PD1DHT1	PD1DHT0	PD1PRE#	PD1DMA#	PD1RDY#	PD1ADV

Bit 7-Bit 6 PD1AST1~0 PD1 Data Register Port (1F0h) Address Setup Time

Definition of these bits same as PD0AST1~0

Bit 5-Bit 4 PD1DHT1~0 PD1 Data Register Port (1F0h) Data Hold Time

Definition of these bits same as PD0DHT1~0

Bit 3 PD1PRE# PD1 Prefetch/Post write control

0 Prefetch/Post write Enable  
1 Prefetch/Post write Disable

Bit 2 PD1DMA#PD1 DMA mode control

0 DMA mode Enable  
1 DMA mode Disable

Bit 1 PD1RDY# PD1 Data Register Port (1F0h) IOCHRDY Control

0 IOCHRDY Enable  
1 IOCHRDY Disable

Bit 0 PD1ADV PD1 Data Register Port (1F0h) Advanced Timing Enable

0 Normal timing  
(depend on SP1,MD1,MD0 setting)  
1 Advanced timing  
(depend on PD1TIM1~0 setting)

CRX8Ch (SD0TIM0) Read/Write Secondary Drive0 Timing Control 0

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SD0ACT3	SD0ACT2	SD0ACT1	SD0ACT0	SD0RCV3	SD0RCV2	SD0RCV1	SD0RCV0

Bit 7-Bit 4 SD0ACT3~0 SD0 Data Register Port (170h) Read/Write Active Time

Definition of these bits same as PD0ACT3~0

Bit 3-Bit 0 SD0RCV3~0 SD0 Data Register Port (170h) Read/Write Recovery Time

Definition of these bits same as PD0RCV3~0

CRX8Dh (SD0TIM1)      Read/Write      Secondary Drive0 Timing Control 1

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SD0AST1	SD0AST0	SD0DHT1	SD0DHT0	SD0PRE#	SD0DMA#	SD0RDY#	SD0ADV

Bit 7-Bit 6 SD0AST1~0      SD0 Data Register Port (170h) Address Setup Time

Definition of these bits same as PD0AST1~0

Bit 5-Bit 4 SD0DHT1~0      SD0 Data Register Port (170h) Data Hold Time

Definition of these bits same as PD0RDHT1~0

Bit 3      SD0PRE#      SD0 Prefetch/Post write control

<u>0</u>	<u>Prefetch/Post write Enable</u>
1	Prefetch/Post write Disable

Bit 2      SD0DMA#SD0 DMA mode control

<u>0</u>	<u>DMA mode Enable</u>
1	DMA mode Disable

Bit 1      SD0RDY#      SD0 Data Register Port (170h) IOCHRDY Control

<u>0</u>	<u>IOCHRDY Enable</u>
1	IOCHRDY Disable

Bit 0      SD0ADV      SD0 Data Register Port (170h) Advanced Timing Enable

<u>0</u>	<u>Normal timing</u> <u>(depend on SP1,MD1,MD0</u> <u>setting)</u>
1	Advanced timing (depend on SD0TIM1~0 setting)

CRX8Eh (SD1TIM0)      Read/Write      Secondary Drive1 Timing Control 0

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SD1ACT3	SD1ACT2	SD1ACT1	SD1ACT0	SD1RCV3	SD1RCV2	SD1RCV1	SD1RCV0

Bit 7-Bit 4 SD1ACT3~0 SD1 Data Register Port (170h) Read/Write Active Time

Definition of these bits same as PD0RCV3~0

Bit 3-Bit 0 SD1RCV3~0 SD1 Data Register Port (170h) Read/Write Recovery Time

Definition of these bits same as PD0RCV3~0

CRX8Fh (SD1TIM1) Read/Write Secondary Drive1 Timing Control 1

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SD1AST1	SD1AST0	SD1DHT1	SD1DHT0	SD1PRE#	SD1DMA#	SD1RDY#	SD1ADV

Bit 7-Bit 6 SD1AST1~0 SD1 Data Register Port (170h) Address Setup Time

Definition of these bits same as PD0RCV3~0

Bit 5-Bit 4 SD1DHT1~0 SD1 Data Register Port (170h) Data Hold Time

Definition of these bits same as PD0RCV3~0

Bit 3 SD1PRE# SD1 Prefetch/Post write control

<u>0</u>	<u>Prefetch/Post write Enable</u>
1	Prefetch/Post write Disable

Bit 2 SD1DMA#SD1 DMA mode control

<u>0</u>	<u>DMA mode Enable</u>
1	DMA mode Disable

Bit 1 SD1RDY# SD1 Data Register Port (170h) IOCHRDY Control

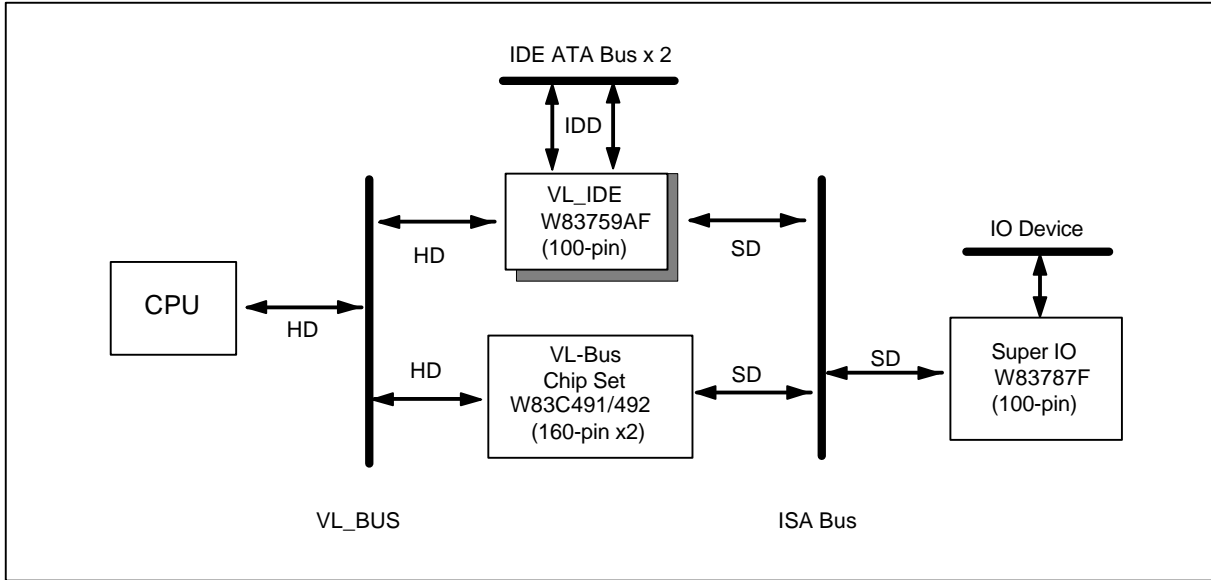
<u>0</u>	<u>IOCHRDY Enable</u>
1	IOCHRDY Disable

Bit 0 SD1ADV SD1 Data Register Port (170h) Advanced Timing Enable

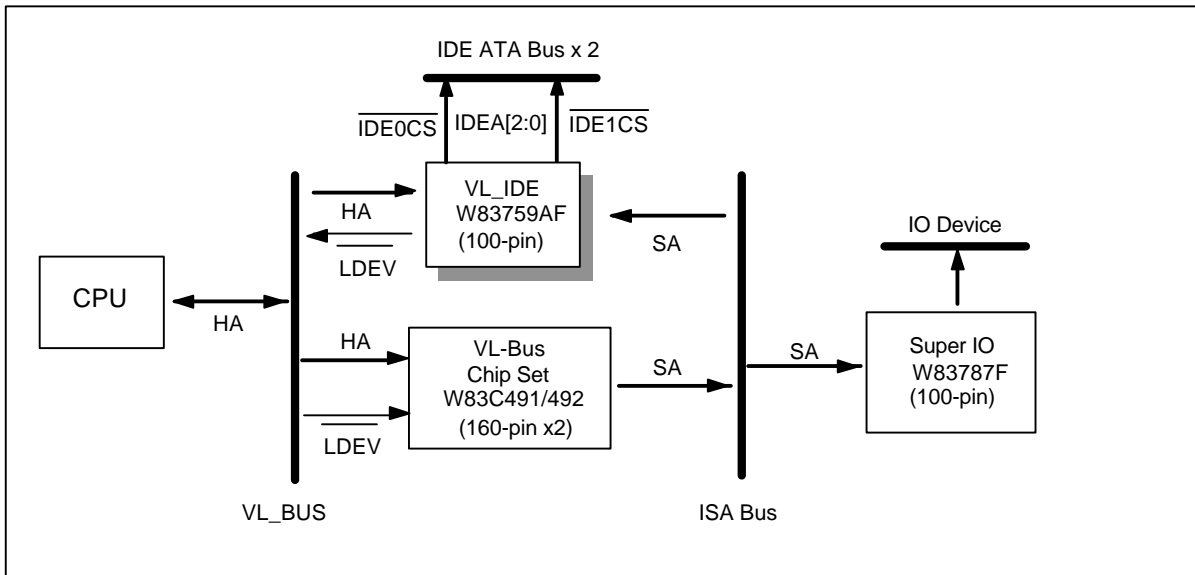
<u>0</u>	<u>Normal timing</u> <u>(depend on SP1,MD1,MD0 setting)</u>
1	Advanced timing (depend on SD1TIM1~0 setting)

**SYSTEM BLOCK DIAGRAM**

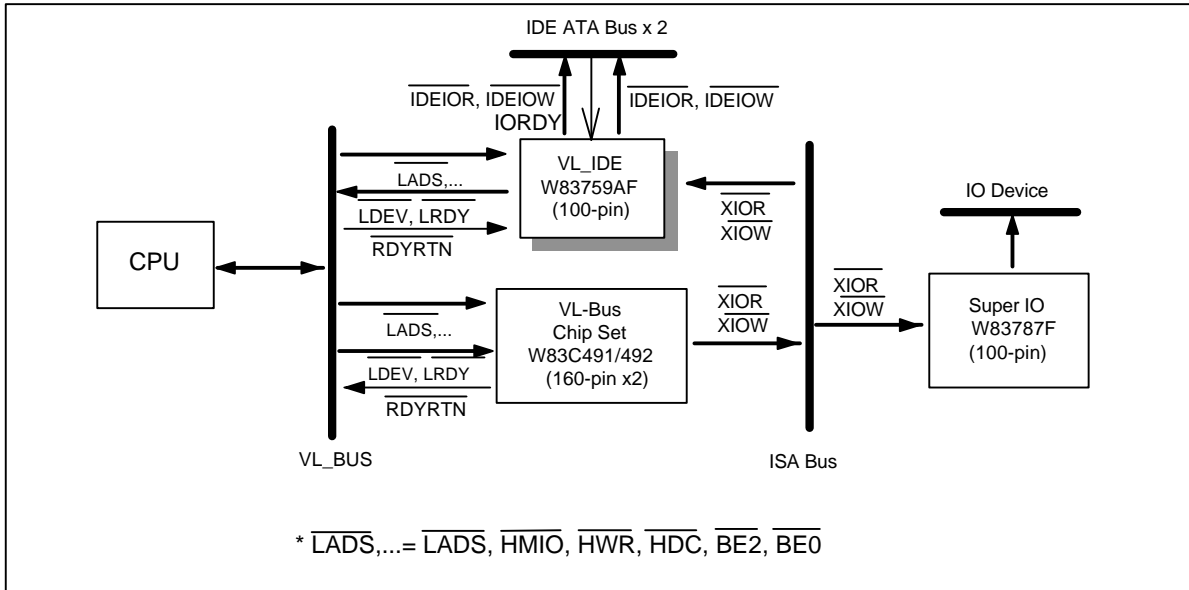
**1. DATA FLOW**



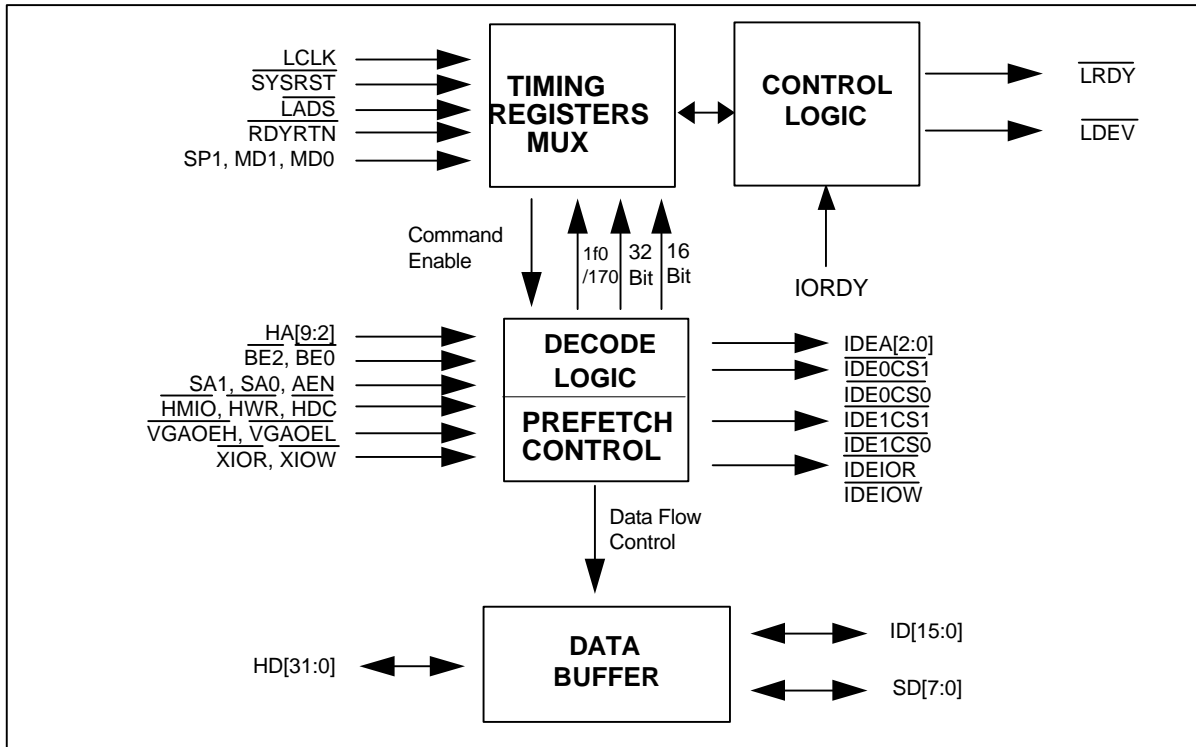
**2. ADDRESS DECODE**



3. CONTROL SIGNAL



FUNCTION BLOCK DIAGRAM



**FUNCTIONAL DESCRIPTION**

**1. RESET INITIALIZATION**

The CPU clock rate, hard disk access time, hard disk controller enable and hard disk I/O select are latched at the rising edge of SYSRST. These values are used to control the host and drive access signal timing.

Additionally, the W83759A is initialized to a known state by an active low on SYSRST. Any operation in progress is immediately terminated by SYSRST.

**2. HOST INTERFACE**

The W83759A operates as a slave device, responding only to cycles within the host I/O address space. The IDE drive data port at address 1F0h is a 16-bit port that requests a double-word data transfer at address 1F0h. All byte swapping, conversion, word and double-word assembly are done at the host interface. Table 1 summarizes the W83759A host interface cycle decoding.

Table 1 W83759A Cycle Definition

HMIO	HDC	HWR	ADDRESS SPACE	HOST BUS CYCLE	W83759A CYCLE
0	1	0	1F0h-1F7h and 3F6h	I/O Read	IDE0 Read Cycle
0	1	1	1F0h-1F7h and 3F6h	I/O Write	IDE0 Write Cycle

0	1	0	170h-177h and 376h	I/O Read	IDE1 Read Cycle
0	1	1	170h-177h and 376h	I/O Write	IDE1 Write Cycle

**a. CPU WRITE CYCLES**

Table 2 W83759A Write Data Operation

BYTE ENABLE				W83759A INPUT DATA			I/O ADDRESS
BE3	BE2	BE1	BE0	HD[31:16]	HD[15:0]	SD[7:0]	
1	1	1	0	×	×	Valid	1F1-1F7(171-177)
1	1	0	1	×	×	Valid	
1	0	1	1	×	×	Valid	
0	1	1	1	×	×	Valid	
1	1	0	0	×	Valid	×	1F0 (170)
0	0	0	0	Valid	Valid	×	

8-bit IDE Write Data Path:

CPU → Valid HD Byte → SD[7:0] → W83759A → ID[7:0]

16/32-bit IDE Write Data Path:

CPU → Valid HD Word → W83759A → ID[15:0]

**b. CPU READ CYCLES**

Table 3 W83759A Read Data Operation

BYTE ENABLE				W83759 OUTPUT DATA			I/O ADDRESS
BE3	BE2	BE1	BE0	HD[31:16]	HD[15:0]	SD[7:0]	
1	1	1	0	×	×	Valid	1F1-1F7(171-177)
1	1	0	1	×	×	Valid	
1	0	1	1	×	×	Valid	
0	1	1	1	×	×	Valid	
1	1	0	0	×	Valid	×	1F0 (170)
0	0	0	0	Valid	Valid	×	

8-bit IDE Read Data Path:

CPU → Valid HD Byte → Chip Set → SD[7:0] → W83759A → ID[7:0]

16/32-bit IDE Read Data Path:

CPU → Valid HD Word → W83759A → ID[15:0]

**3. DRIVE INTERFACE**

The W83759A is designed to work with standard IDE disk drives. For the IDE interface, the W83759A provides a 16-bit data path ID[15:0], address lines IDEA[2:0], decoded device select signals IDE0CS0 ( IDE1CS0 ) and IDE0CS1 ( IDE1CS1 ), and decoded command signals IDEIOR and IDEIOW .

During normal operation, the drive address outputs IDEA[2:0] are used to select a register in an IDE drive. These addresses are generated from BE2, BE0, HA2 and SA1, SA0. Table 4 summarizes the type enable decoding for normal operation.

Table 4 IDEA[2:0] Generation

<u>HA2</u>	<u>BE2</u>	<u>BE0</u>	<u>SA1</u>	<u>SA0</u>	<u>IDEA[2:0]</u>	<u>I/O ADDRESS</u>
0	1	0	×	×	000	1F0(170) 16-bit
0	0	0	×	×	000	1F0(170) 32-bit
0	×	×	0	1	001	1F1(171)
0	×	×	1	0	010	1F2(172)
0	×	×	1	1	011	1F3(173)
1	×	×	0	0	100	1F4(174)
1	×	×	0	1	101	1F5(175)
1	×	×	1	0	110	1F6(176)
1	×	×	1	1	111	1F7(177)

Two drive chip select signals, IDE0CS0 ( IDE1CS0 ) and IDE0CS1 ( IDE1CS1 ), are generated from the local bus addresses and ISA bus address. The 16-bit data register may be read or written at I/O address 1F0h(170h). The 8-bit IDE command and status registers are at I/O addresses 1F1h through 1F7h(and 171h through 177h). The IDEIOR or IDEIOW commands are generated for all address regions in which IDE0CS0 ( IDE1CS0 ) and IDE0CS1 ( IDE1CS1 ) are active. Table 5 summarizes the decoding of these signals.

Table 5 Drive Select Signal Operation

<u>SELECT SIGNAL</u>	<u>ADDRESS RANGE</u>
<u>IDE0CS0</u>	I/O Address 1F0h through 1F7h
<u>IDE0CS1</u>	I/O Address 3F6h
<u>IDE1CS0</u>	I/O Address 170h through 177h
<u>IDE1CS1</u>	I/O Address 376h

#### 4. IDE TIMING CONTROL

Pin SP1 is used to set the VL-Bus speed. The IDE drive interface will maintain the same ATA PIO timing parameters for IDE drive 16-bit IO access cycles (1F0/170) regardless of whether the VL-Bus operates at 33 or 50 MHz.

In W83759 mode, IDE drive timing is controlled by pins MD1 and MD0 , which are used to select the IDE drive PIO mode 0-2. The drive timing depends on the ATA specification for the IDE drive PIO mode selected.

In W83759A mode, IDE drive timing is controlled by pins EMD1 and EMD0 , which are used to select the IDE drive PIO mode 2-4. The drive timing depends on the ATA specification for the IDE drive PIO mode selected.

Table 6 summarizes the ATA Rev.4.0 and ATA-2 PIO timing parameters.

Table 7 and Table 8 summarizes the W83759A PIO read/write command pulse and cycle timing when 16-bit IDE IO access is performed. Because 8-bit IDE IO accesses are always passed to the ISA bus, the W83759A transceives data through the ISA data bus and induces IDE read/write

commands from ISA XIOR/XIOW. Thus the 8-bit command timing will always meet ATA timing specifications.

Table 6 ATA Rev. 4.0 and ATA-2 PIO Minimum Timing Parameters

Unit : ns

ATA PIO	Mode 4		Mode 3		Mode 2		Mode 1		Mode 0	
	Active Pulse	Cycle Time	Active Pulse	Cycle Time	Active Pulse	Cycle Time	Active Pulse	Cycle Time	Active Pulse	Cycle Time
16-bit	60	120	80	180	100	240	125	383	165	600
8-bit	60	120	80	180	290	290	290	383	290	600

Table 7 In W83759 mode, PIO Command Pulse and Cycle Timing

Unit :LCLK

SP1	MD1	MD0	IDE WRITE ACTIVE PULSE	IDE READ ACTIVE PULSE	READ/WRITE CYCLE TIME	IDE Mode SELECT
0	0	0	6 (180)	7 (210)	22 (660)	Mode 0
0	0	1	6 (180)	7 (210)	19 (570)	Mode 0+
0	1	0	8 (240)	9 (270)	13 (390)	Mode 1
0	1	1	4 (120)	5 (150)	9 (270)	Mode 2
1	0	0	9 (180)	10 (200)	31 (620)	Mode 0
1	0	1	9 (180)	10 (200)	27 (540)	Mode 0+
1	1	0	7 (140)	8 (160)	19 (380)	Mode 1
1	1	1	6 (120)	7 (140)	13 (260)	Mode 2

Note : It is recommended that SP be set to 0 when LCLK is 33 MHz. The initial default value is SP1=0. The timing value (nS) is based on LCLK=20 nS when SP1=1 and LCLK=30 nS when SP1=0.

Table 8 In W83759A mode, PIO Command Pulse and Cycle Timing

Unit :LCLK

SP1	EMD 1	EMD 0	IDE WRITE ACTIVE PULSE	IDE READ ACTIVE PULSE	READ/WRITE CYCLE TIME	IDE Mode SELECT
0	0	0	4 (120)	5 (150)	8 (240)	Mode 2
0	0	1	3 (90)	4 (120)	6 (180)	Mode 3
0	1	0	3 (90)	4 (120)	6 (180)	Mode 3
0	1	1	2 (60)	3 (90)	4 (120)	Mode 4
1	0	0	4 (80)	5 (100)	11 (220)	Mode 2
1	0	1	4 (80)	5 (100)	9 (180)	Mode 3
1	1	0	3 (60)	4 (80)	7 (140)	Mode 4-
1	1	1	2 (40)	3 (60)	5 (100)	Mode 4+

Note : It is recommended that SP be set to 0 when LCLK is 33 MHz. The initial default value is SP1=0. The timing value (nS) is based on LCLK=20 nS when SP1=1 and LCLK=30 nS when SP1=0.

## 5. Prefetch Control

The W83759A IDE command prefetch feature provides concurrent operations by pipelined read-ahead the next data word(s) from the drive while the host is transferring previously requested disk data into system memory. This will reduce the amount of time that the host must pause and wait for data to be access. While the host is writing data to memory the W83759A is simultaneously reading data from the disk drive. As soon as the host reads the W83759A data, new data is requested by W83759A from the disk drive. This prefetch feature is only active for disk data at the 1F0h and 170h IO address and do not operate on other disk register data.

## 6. Power-saving Control

The W83759A provides three levels of power-saving mode to reduce the power consumption for Green PC. The most lightly power-saving mode is that all of the drive's control, address, data and other signals go to a logic 1 level standby state when no IDE disk cycle is active. This will reduce the unnecessary power and decrease the amounts of EMI radiation which is generated by continually driving the long IDE cable.

After power on, the W83759A automatically enters the "Auto-Power-Down" mode. In this mode the only active logic inside the W83759A is the host address decoder and bus tracking state machine. This power saving is obtained by not switching logic inside the W83759A that is not being utilized. Whenever the IDE transfer cycle is detected, the W83759A leaves APD mode and all of the chip is active. The W83759A enters APD mode again after the completion of an IDE transfer cycle.

With supporting the deep green scheme, the W83759A provides advanced power saving modes which are standby mode and suspend mode. When standby mode enables (STBY# bit is low), all of the logic inside the W83759A is stop until standby mode disables (STBY# bit is high). When suspend mode enables (SUSPEN bit is high and  $\overline{DMASL}$  is low on  $\overline{SYSRST}$  rising) the W83759A will enter suspend state while  $\overline{SUSP}$  is low and resume to normal state while  $\overline{SUSP}$  is high.

**ABSOLUTE MAXIMUM RATINGS**

( $V_{DD} = 5V \pm 5\%$ ,  $V_{SS} = 0V$ )

PARAMETER	RATING	UNIT
Power Supply Voltage	-0.3 to 7.0	V
Input Voltage	$V_{SS} - 0.3$ to $V_{DD} + 0.3$	V
Operating Temperature (Ta)	0 to + 70	°C
Storage Temperature	-55 to + 150	°C

**DC CHARACTERISTICS**

( $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ,  $V_{DD} = 5V \pm 5\%$ ,  $V_{SS} = 0V$ )

PARAMETER	SYMBOL	MIN	MAX	UNIT	CONDITIONS
Input Low Voltage	$V_{IL}$	-0.3	0.8	V	
Input High Voltage	$V_{IH}$	2.0	$V_{DD} + 0.3$	V	
Input High Leakage with Pull-Down	$I_{LIHD}$	-	+500	$\mu\text{A}$	$V_{IN} = V_{DD}$
Input Low Leakage with Pull-Up	$I_{LILU}$	-	-500	$\mu\text{A}$	$V_{IN} = 0V$
Input High Leakage	$I_{LIH}$	-	+10	$\mu\text{A}$	$V_{IN} = V_{DD}$

Input Low Leakage	$I_{LIL}$	-	-10	$\mu\text{A}$	$V_{IN} = 0\text{V}$
Output Low Voltage	$V_{OL}$	-	0.4	V	$I_{OL} = 8\text{mA}$ (LDEV ,SD,IDE pins) $I_{OL} = 6\text{mA}$ (other pins)
Output High Voltage	$V_{OH}$	2.4	$V_{DD}$	V	$I_{OL} = -8\text{mA}$ (LDEV ,SD,IDE pins) $I_{OL} = -6\text{mA}$ (other pins)
Input Capacitance	$C_{IN}$	-	5	pF	
Output Capacitance	$C_{OUT}$	-	10	pF	
Operating Current	$I_{DD}$	-	25	mA	$F_{LCLK} = 50\text{MHz}$
Standby Current	$I_{STBY}$	-	800	$\mu\text{A}$	All input and I/O pins pulled high, LCLK = $V_{DD}$

## AC CHARACTERISTICS

All AC timing is measured from the 0.8V and 2.0V on the source signal to the 0.8V and 2.0V level on the signal under test.

AC specifications are given for the following testing conditions:

$V_{DD} = 5\text{V} \pm 5\%$ , Temp. =  $0^\circ\text{C}$  to  $70^\circ\text{C}$

VL-Bus shared signal loading = 100pF

VL-Bus non-shared signal loading = 33pF

ISA Bus signal loading = 240pF

IDE device interface loading = 30pF

SYMBOL	PARAMETER	MIN.	MAX	UNIT	FIG.
t1	LCLK Period	20	-	nS	Fig. 1
t2	LCLK High Time	5	-	nS	Fig. 1
t3	LCLK Low Time	5	-	nS	Fig. 1
t4	$\overline{\text{SYSRST}}$ Pulse Width	16	-	LCLK	Fig. 1
t5	POS Pin to $\overline{\text{SYSRST}}$ Setup Time	200	-	nS	Fig. 1
t6	POS Pin Hold Time from $\overline{\text{SYSRST}}$	10	-	nS	Fig. 1
t7	$\overline{\text{LADS}}$ to LCLK Setup Time	6	-	nS	Fig. 2
t8	$\overline{\text{LADS}}$ Hold Time from LCLK	3	-	nS	Fig. 2
t9	LDEV Active Delay from Address	3	9	nS	Fig. 2
t10	VESA IO Read Host Data Drive Delay	5	16	nS	Fig. 2,4
t11	$\overline{\text{HMIO}}$ , $\overline{\text{HDC}}$ , $\overline{\text{HWR}}$ to LCLK Setup Time when LDEV asserted at T2	5	-	nS	Fig. 2,3

t12	$\overline{\text{HMIO}}, \overline{\text{HDC}}, \overline{\text{HWR}}$ to LCLK Setup Time when LDEV asserted at T2	10	-	nS	Fig. 2,3
t13	LRDY Active Delay from LCLK	5	16	nS	Fig. 2,3
t14	LRDY Inactive Delay from LCLK	6	18	nS	Fig. 2,3
t15	RDYRTN to LCLK Setup Time	6	-	nS	Fig. 2,3
t16	RDYRTN Hold Time from LCLK	3	-	nS	Fig. 2,3
t17	VESA IO Write Host Data Valid Delay	-	20	nS	Fig. 3
t18	VESA IO Write Host Data Hold Time	0	-	nS	Fig. 3,5
t19	IDEA[2:0] Valid Delay from Address Valid	-	18	nS	Fig. 4,5
t20	IDEA[2:0] Invalid Delay from Address Change	5	18	nS	Fig. 4,5
t21	IDE0CS0, IDE1CS0 Valid Delay from Address valid	-	18	nS	Fig. 4,5
t22	IDE0CS0, IDE1CS0 Invalid Delay from Address Change	5	18	nS	Fig. 4,5
t23	IDEIOR, IDEIOW Active Delay from LCLK	-	22	nS	Fig. 4,5
t24	IDEIOR, IDEIOW Inactive Delay from LCLK	-	24	nS	Fig. 4,5
t25	IDE Read IDD Data Hold Time from LCLK	0	-	nS	Fig.4
t26	IDE Read IDD to HD Delay	-	16	nS	Fig.4
t27	IDE Read HD Float Delay from LCLK	10	30	nS	Fig.4
t28	IDE Write IDD Drive Delay	-	20	nS	Fig.5
t29	IDE Write IDD Float Delay	10	30	nS	Fig.5
t30	IDEA[2:0] Valid Delay from A2, SA[1:0] Valid	-	20	nS	Fig.6,7
t31	IDEA[2:0] Invalid Delay from A2, SA[1:0] Change	5	20	nS	Fig.6,7
t32	IDE0CS1, IDE1CS1 Valid Delay from Address Valid	-	17	nS	Fig.6,7
t33	IDE0CS1, IDE1CS1 Invalid Delay from Address Change	4	17	nS	Fig.6,7
t34	ISA IDE Read IDD to SD Delay	8	18	nS	Fig.6
t35	ISA IDE Read IDD Data Hold Time from IDEIOR	5	-	nS	Fig.6
t36	ISA IDE Write SD to IDD Delay	8	18	nS	Fig.7
t37	ISA IDE Write SD Data Hold Time from XIOW	30	-	nS	Fig.7
t38	VGA Read IDD to HD Delay	-	16	nS	Fig.8
t39	VGA Read HD Float Delay from VGAOEL	-	20	nS	Fig.8
t40	VGA Write HD to IDD Delay	-	16	nS	Fig.9

t41	VGA Write HD Float Delay from $\overline{\text{VGAOE}}\overline{\text{H}}$	-	20	nS	Fig.9
t42	ISA IDD Read $\overline{\text{IDEIOR}}$ Active Delay from $\overline{\text{XIOR}}$	-	20	nS	Fig.6
t43	ISA IDD Read $\overline{\text{IDEIOR}}$ Inactive Delay from $\overline{\text{XIOR}}$	-	20	nS	Fig.6
t44	ISA IDE Write $\overline{\text{IDEIOW}}$ Active Delay from $\overline{\text{XIOW}}$	-	20	nS	Fig.7
t45	ISA IDE Write $\overline{\text{IDEIOW}}$ Inactive Delay from $\overline{\text{XIOW}}$	-	20	nS	Fig.7

**TIMING WAVEFORMS**

All AC timing is measured from the 0.8V and 2.0V on the source signal to the 0.8V and 2.0V level on the signal under test.

**1. LCLK,  $\overline{\text{SYSRST}}$ , TIMING**

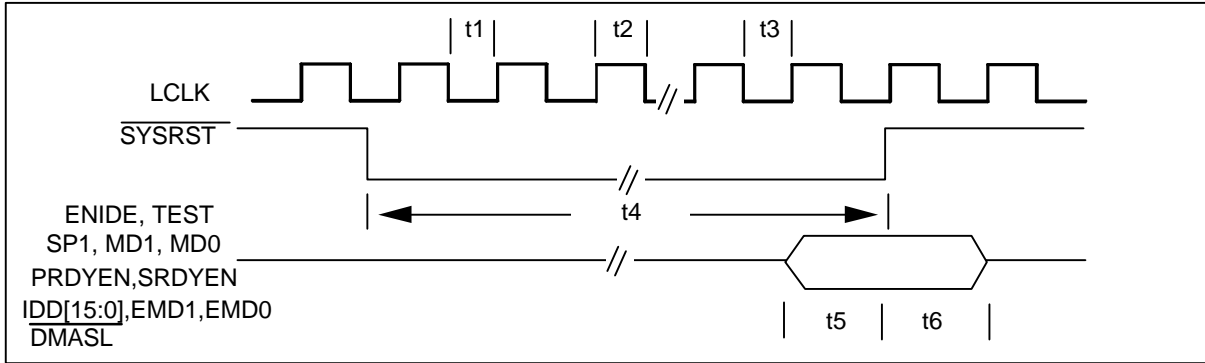


Fig. 1

Note : ENIDE, TEST, SP1, MD1, MD0, PRDYEN, SRDYEN, IDD[15:0], EMD1, EMD0,  $\overline{\text{DMASL}}$  are POS (Power-On Setting) pins. When  $\overline{\text{SYSRST}}$  is low they are tri-stated as inputs.

**2. VESA IO READ TIMING**

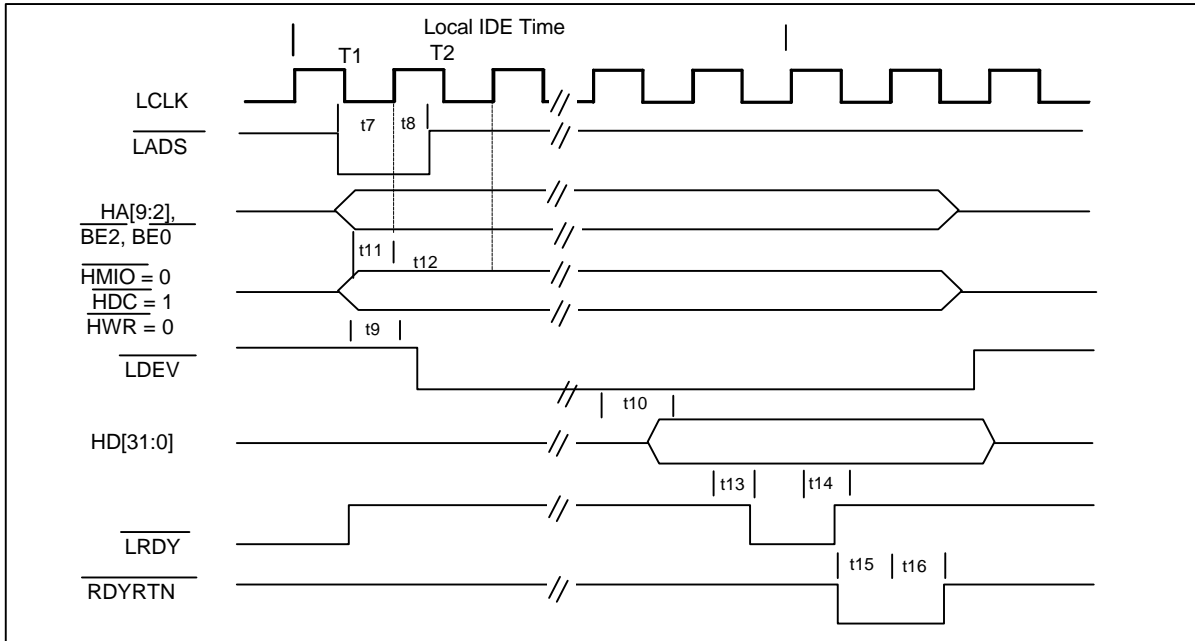
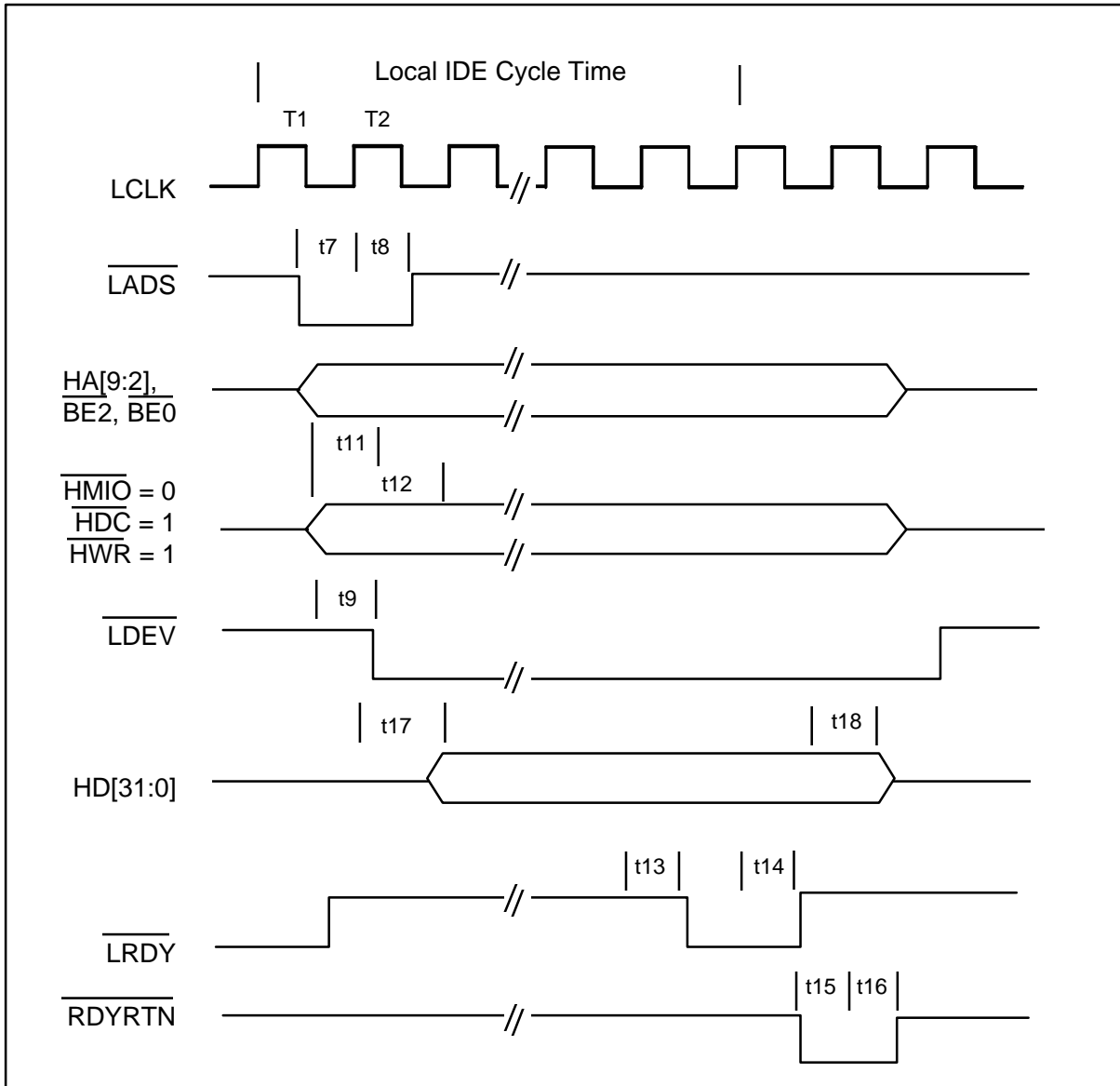


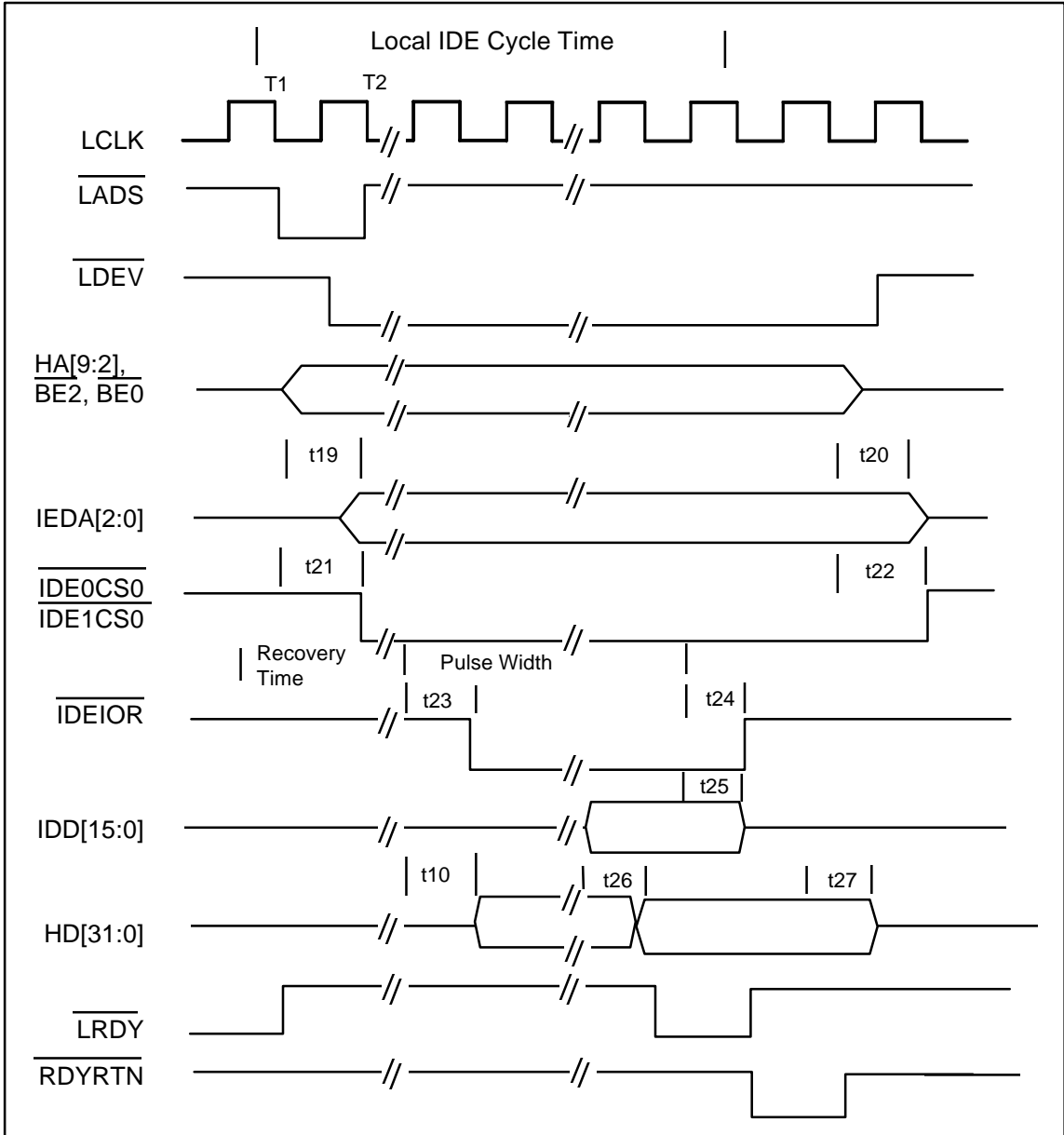
Fig. 2

Note : Local IDE cycle time is determined by SP1, MD1, and MD0 or by SP1, EMD1 and EMD0 at power on. After power on the driver can program timing register to tune a best timing.

3. VESA IO WRITE TIMING



4. IDE IO READ TIMING



Note : The recovery time and pulse width are determined by SP1, MD1, and MD0, or EMD1 and EMD0 as indicated Table 7. and Table 8.

Example: When SP = 1 and MD1 = MD0 = 0, the IDEIOR pulse width is 10 LCLK and recovery time is 21 LCLK (cycle time is 31 LCLK).

5. IDE IO Write Timing

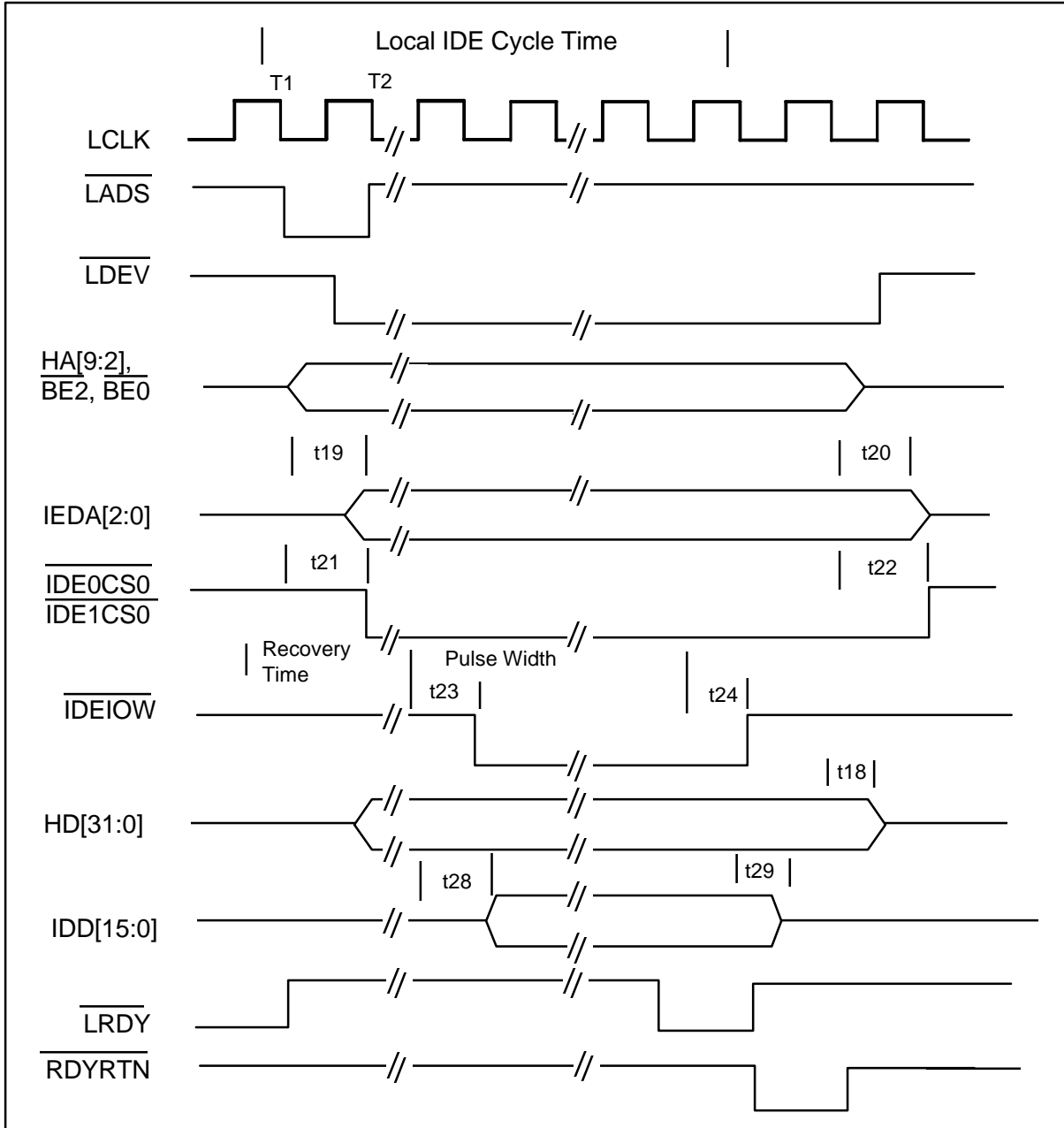


Fig: 5

Note : The recovery time and pulse width are determined by SP1, MD1, MD0,EMD1,EMD0 as indicated in Table 7 and Table 8.

Example : When SP = 1 and MD1 = MD0 = 0, the  $\overline{\text{IDEIOW}}$  pulse width is 9 LCLK and recovery time is 22 LCLK (cycle time is 31 LCLK).

6. ISA IO READ TIMING

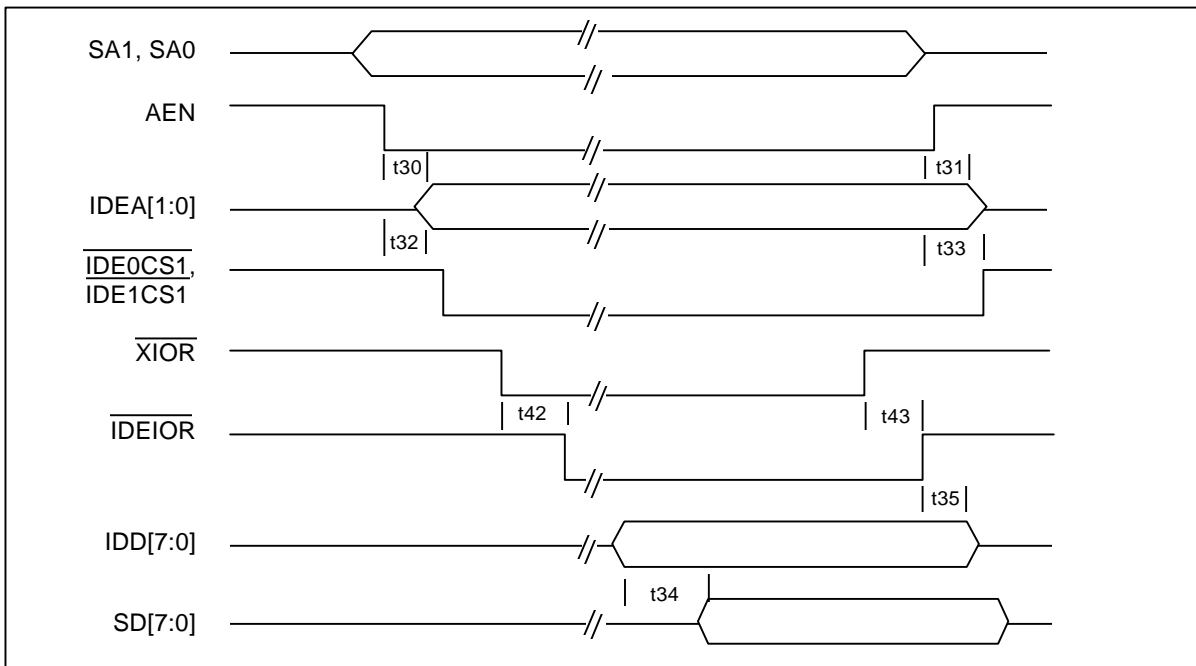


Fig. 6

**7. ISA IO WRITE TIMING**

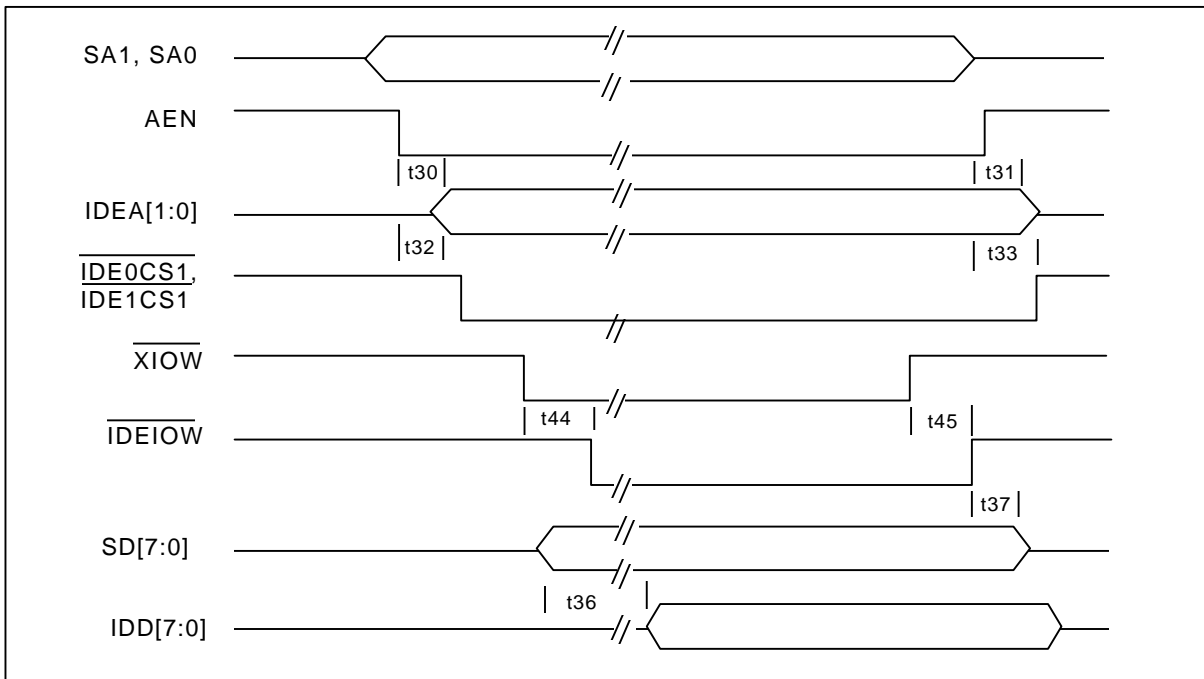


Fig 7

**8. VGAOEL READ TIMING**

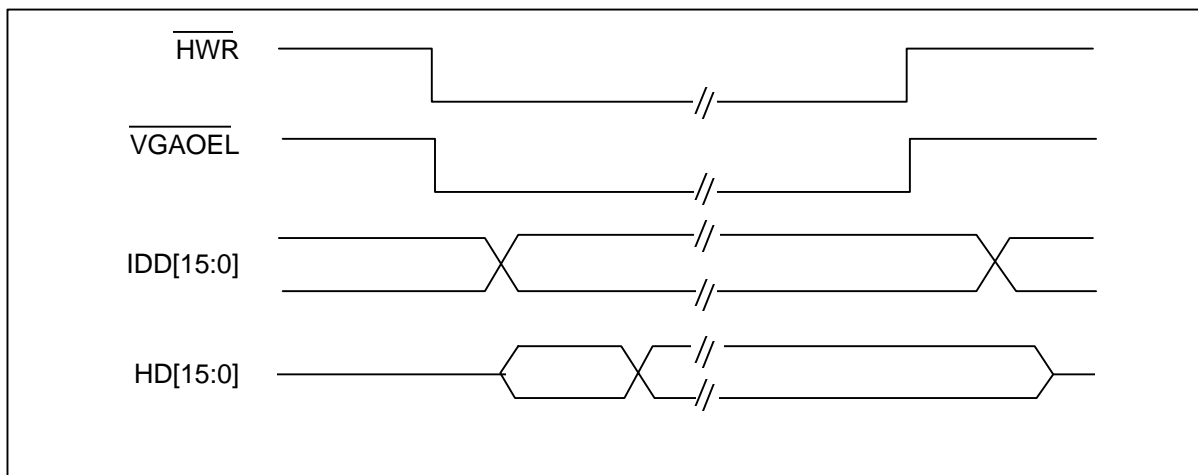


Fig. 8

**9. VGAOEH WRITE TIMING**

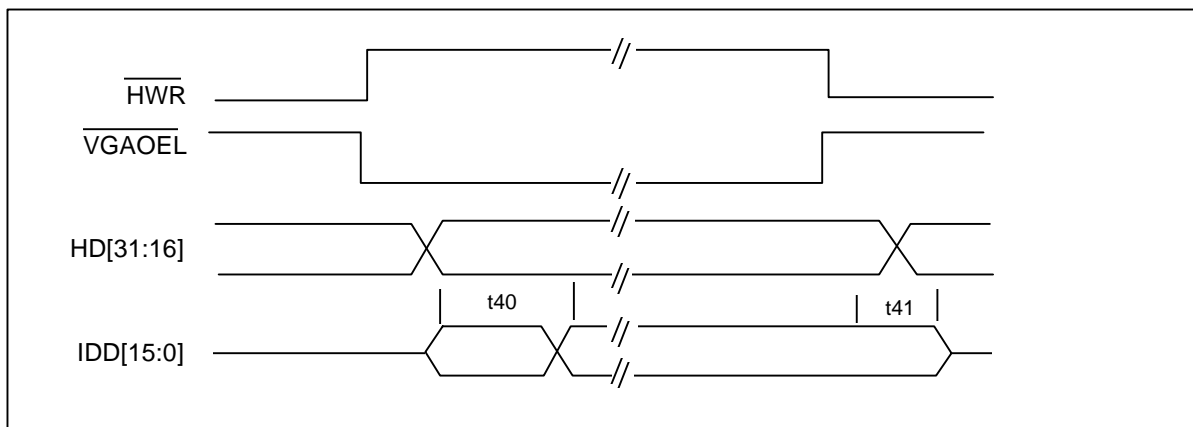
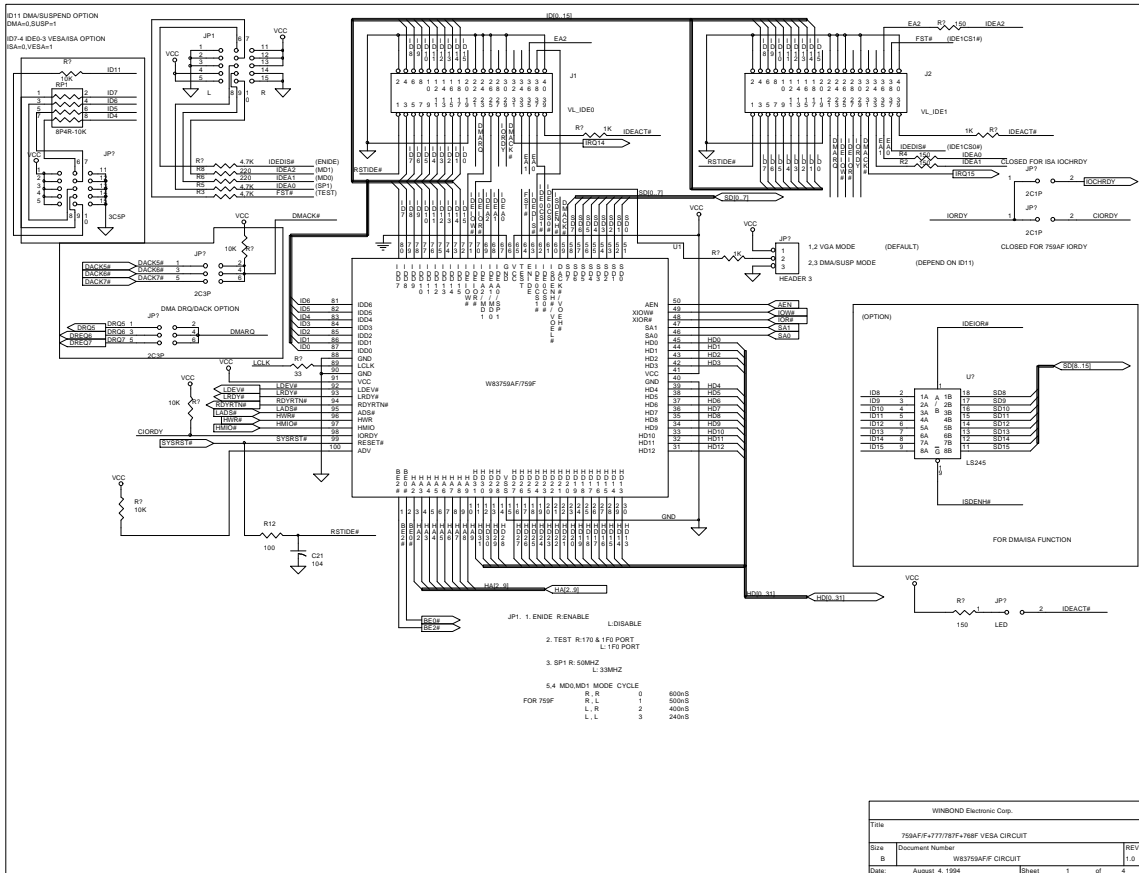
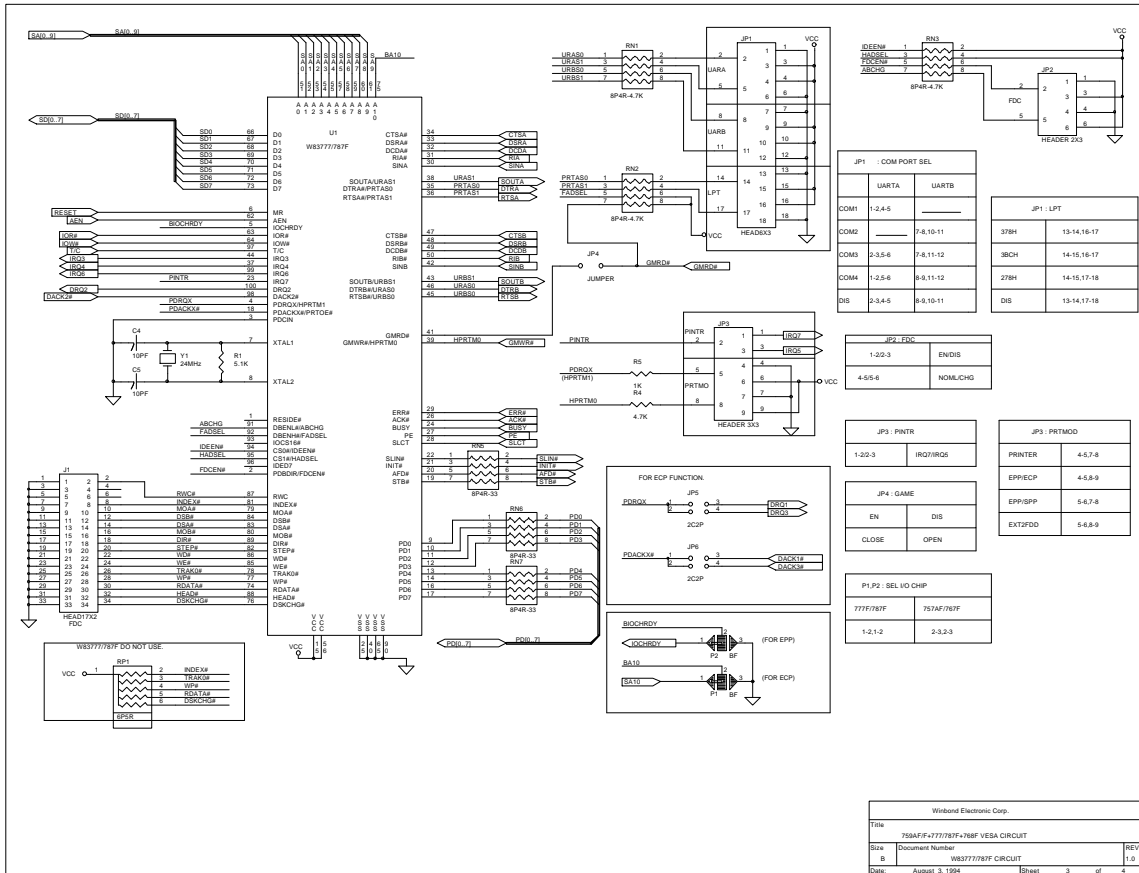


Fig. 9

**APPLICATION CIRCUIT**









PACKAGE INFORMATION

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.130	—	—	3.30
A <sub>1</sub>	0.004	—	—	0.10	—	—
A <sub>2</sub>	0.107	0.112	0.117	2.73	2.85	2.97
b	0.010	0.012	0.016	0.25	0.30	0.40
c	0.004	0.006	0.010	0.10	0.15	0.25
D	0.546	0.551	0.556	13.87	14.00	14.13
E	0.782	0.787	0.792	19.87	20.00	20.13
[E]	0.020	0.026	0.032	0.50	0.65	0.80
H <sub>D</sub>	0.728	0.740	0.752	18.49	18.80	19.10
H <sub>E</sub>	0.954	0.976	0.988	24.49	24.80	25.10
L	0.039	0.047	0.055	1.00	1.20	1.40
L <sub>1</sub>	0.087	0.094	0.103	2.21	2.40	2.62
y	—	—	0.004	—	—	0.10
φ	0°	—	12°	0°	—	12°

Note:  
 1.Dimension D & E do not include interlead flash.  
 2.Dimension b does not include dambar protrusion/intrusion.  
 3.Controlling dimension : Millimeter.  
 4.General appearance spec. should be based on final visual inspection spec.

TITLE:	100LD QFP(14X20mm) -A42 L/F, FOOTPRINT	PACKAGE OUTLINE 4.8mm
LEADFRAME MATERIAL:	ALLOY 42	
APPR.		DWG NO. Q100-SW1
R&D		REV NO. B
Q.M		SCALE
CHK.		DATE
DEN.	Aven Loin	SHT NO. 1/1

REV NO	DESCRIPTION	DATE
B	1.Update form in the metric system. 2.The effective decimal 0.xx instead of 0.xxx 3.Cancel G & G's dimension.	Feb,01

COPY CONTROLLED