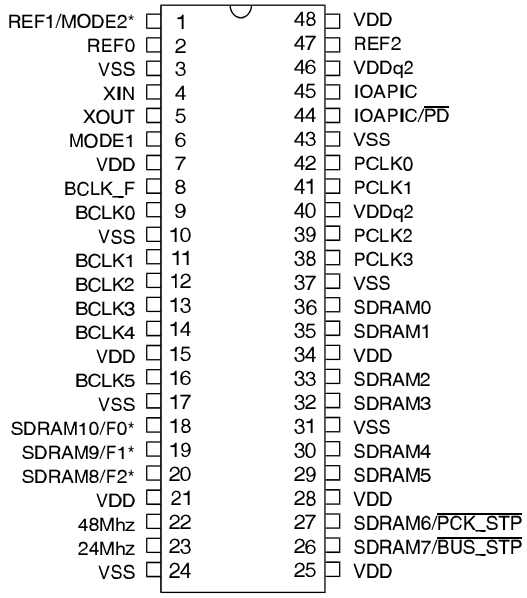
Pentium/SDRAM Clock Generator with Integrated Buffers

FEATURES

- Generates all clock frequencies for Pentium, Pentium PRO, AMD and Cyrix system requiring multiple CPU clocks (SDRAM, Shared memory architecture).
- Supports up to15 Synchronous CPU clocks.
- 7 PCI BUS clocks at synchronous (1/2 of CPU speed) or asynchronous (32Mhz) mode.
- Three 14.318Mhz reference clocks.
- One 24Mhz floppy clock and one 48Mhz USB clock.
- Provide two IOAPIC buffered reference clocks.
- Power management control pins to stop CPU or BUS clocks or power down.
- Mixed voltage support from 3.0 to 5V or (VDDq2=2.5V)
- Available in 300mil 48 pin SSOP.

PIN INFORMATION



PLL52C62-01

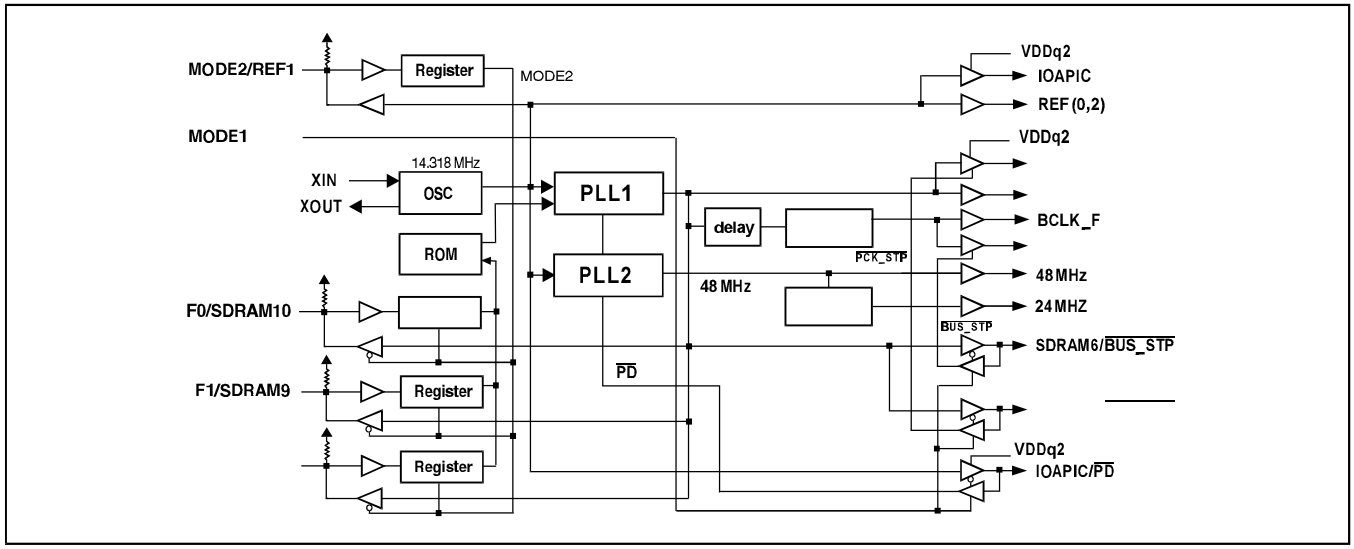
FREQUENCY SELECTION (MHz)

F2	F1	F0	PCLK/SDRAM	BCLK
1	0	0	55	27.5
1	0	1	75	37.5
1	1	0	60.0	30.0
1	1	1	66.6	33.3
0	0	0	83	32 (Asyn)
0	0	1	75	32 (Asyn)
0	1	0	61.6	30.8
0	1	1	68.4	34.2

I/O MODE CONFIGURATION

MODE2	MODE1	PIN18,19,20	PIN26,27,44
1	1	INPUT	OUTPUT
1	0	INPUT	INPUT
0	1	BIDIRECTION	OUTPUT
0	0	BIDITECTION	INPUT

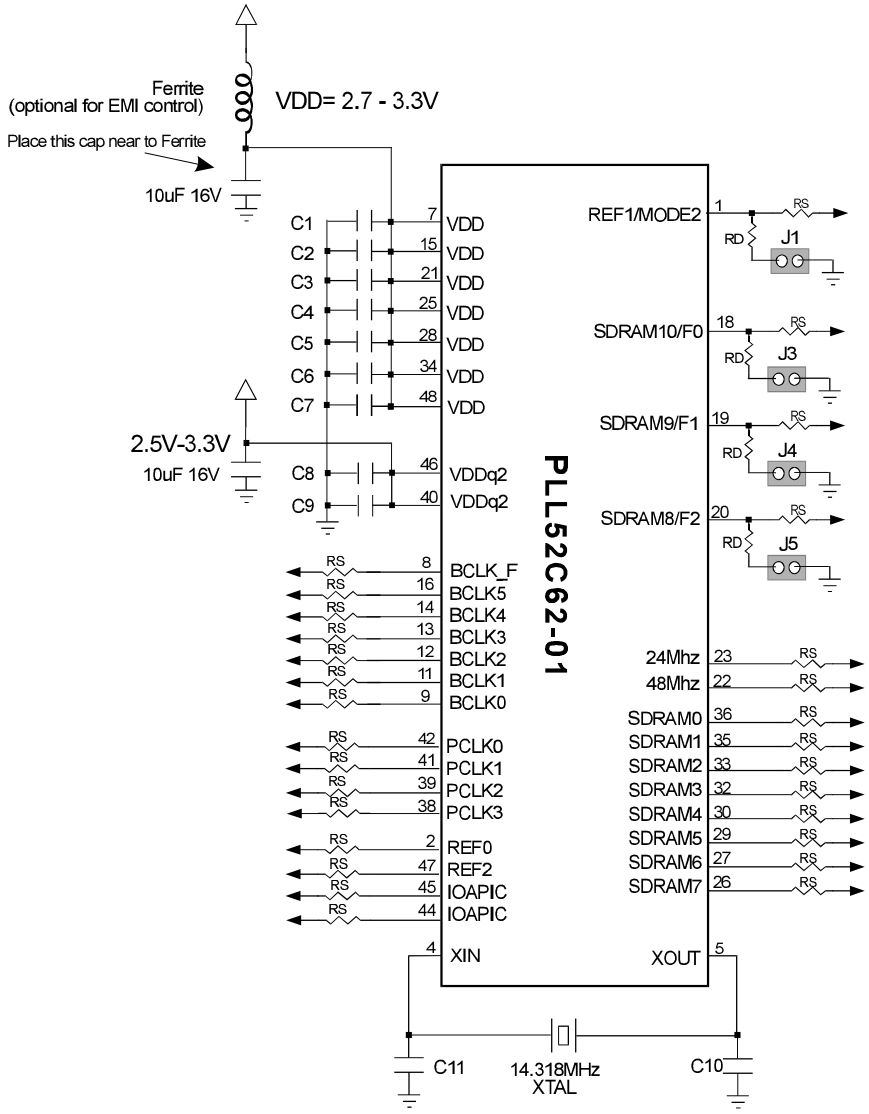
BLOCK DIAGRAM



SIGNAL DESCRIPTIONS

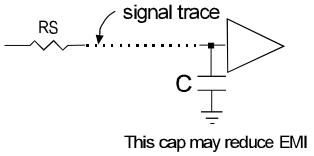
NAME	PIN NUMBER	PIN TYPE	DESCRIPTION
VDD	7,15,21 25,28,34,48	P	Power supply (3V ~ 5V)
VDDq2	40,46	P	Power supply 2.5V-5V
VSS	3,10,17,24 31,37,43	P	Ground
XIN	4	I	14.318Mhz crystal input to be connected to one end of the crystal. This input can also be connected directly to other available source of 14.318Mhz from the PC board.
XOUT	5	O	14.318Mhz crystal output
MODE1	6	I	When HIGH, Pin 26,27 and 44 will be OUTPUT. When LOW, they are INPUT.
REF1/MODE2	1	B	At power-up, these pins act as input and the default value are HIGH. If any of these pins is connected to a pull down of 10K ohm resistor, the input value will be considered as LOW. After the input sampling, these pins will generate output clocks. When MODE2 is LOW pin 18.19 and 20 are Bidirectional , when MODE2 is HIGH they are strictly inputs.
F0/SDRAM10	18		
F1/SDRAM9	19		
F2/SDRAM8	20		
F0	18	I	When MODE2 is HIGH, these pins are inputs for CPU frequencies selections
F1	19		
F2	20		
SDRAM7	26	O	Generates CPU clock for SDRAM applications when MODE1 is HIGH
$\overline{\text{BUS\_STP}}$		I	When MODE1 is LOW and $\overline{\text{BUS\_STP}}$ goes LOW, all BCLK will be LOW
SDRAM6	27	O	Generates CPU clock for SDRAM applications when MODE1 is HIGH
$\overline{\text{PCLK\_STP}}$		I	when MODE1 is LOW and $\overline{\text{PCLK\_STP}}$ goes LOW, all PCLK will be LOW.
IOAPIC	44	O	Buffered reference clock for IOAPIC when MODE1 is HIGH
$\overline{\text{PD}}$		I	When MODE1 is LOW and $\overline{\text{PD}}$ goes LOW, the entire chip will be powered down (All output will be LOW) except BCLK_F.
BCLK(0:5), BCLK_F	9,11,12, 13,14,16,8	O	PCI Bus clocks with frequencies defined by Frequency Table. These pins except BLCK_F will be LOW when BUS_STP is LOW or PD is LOW
PCLK(0:3)	38,39,41,42	O	CPU clocks with frequencies defined by Frequency Table. These pins are LOW when PCK_STP is LOW or PD is LOW
SDRAM(0:5)	36,35,33, 32,330,29	O	SDRAM clocks with frequencies defined by Frequency Table. These pins are LOW when PD is LOW
48MHZ	22	O	48MHZ output for USB
24MHZ	23	O	24MHZ output for SuperIO applications.
REF0,REF2	2,47	O	Buffered reference clock output
IOAPIC	45	O	Reference clock output for parallel processing.

APPLICATION CIRCUITS FOR P52C62-01



Notes:

1. J1:I/O Mode configuration jumper
2. J3-J5: Frequency selection jumpers
3. C10-C11: (optional) for fine tuning the crystal frequency.
4. RS: Series clock terminating resistor is recommended using 22 ohm resistor. To further reduce signal ringing and EMI, a capacitor could be placed near the receiving end of the clock line. (as the drawing shows)



5. C1-C9 are 0.1uF power bypass capacitors, should be placed as close to each VDD pin as physically possible.
6. RD=10K ohm resistor must place near to output pins.

MAXIMUM RATINGS

SUPPLY VOLTAGE	VSS-0.5 TO 7V
INPUT VOLTAGE	VSS-0.5V to VDD+0.5V
ESD VOLTAGE	2000V
POWER DISSIPATION	0.75W

Exposure of the device under conditions beyond the limits specified by Maximum Ratings may cause permanent damage to the device

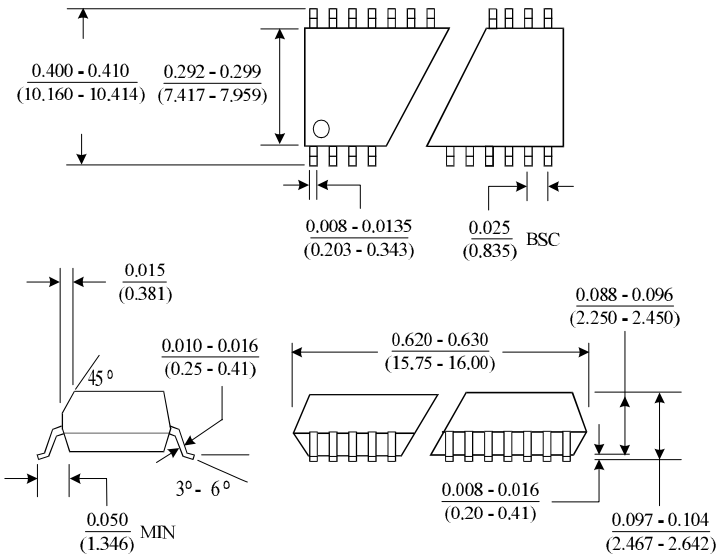
AC SPECIFICATIONS

VDD=3.3V±10% 0°C to 70°C						
PARAMETERS	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Reference input clock rise time	T_{IR}	From 0.8 V to 2V			20	ns
Reference input clock fall time	T_{IF}	From 2V to 0.8V			20	ns
Output rise time	T_{OR}	From 0.8V to 2V 25pF load		1	2	ns
		From 10% to 90% 25pF load		2	4	ns
Output fall time	T_{OF}	From 2V to 0.8V 25pF load		1	2	ns
		From 90% to 10% 25pF load		2	4	ns
Duty cycle	D_T	15pF load.	45	50/50	55	%
Clock Skew (20pF load, @ 1.4V)	T_{SKW}	PCLK to PCLK		50	250	ps
		BCLK to BCLK		90	500	ps
		PCLK to BCLK	1	2	5	ns
Jitter, Absolute (20pF load)	T_{JA}	PCLK, BCLK	-100		100	ps
Jitter, One Sigma (20pF load)	T_{JO}	PCLK, BCLK		50		ps

DC SPECIFICATIONS

VDD=3.3V±10% 0°C to 70°C						
PARAMETERS	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Dynamic Current	I_{DYN}	PCLK at 66.6 MHZ no load		55	110	mA
Static Current	I_{STAT}	All internal circuitry off, XIN=0		25	50	µA
Input High Voltage	V_{IH}	All Inputs except XIN	2			V
Input Low Voltage	V_{IL}	All Inputs except XIN			0.8	V
Output High Current @VOH=2.0V	I_{OH}	PCLK, SDRAM,BCLK		-50		mA
		24Mhz, 48Mhz, REF,IOAPIC		-35		mA
Output Low Current @VOL=0.4V	I_{OL}	PCLK,SDRAM,BCLK		35		mA
		24Mhz, 48Mhz, REF,IOAPIC		25		mA
Pull-up resistor	R_{Pu}	Pin 1,6,18,19,20,26,27,44		25		Kohm
Output Impedance	R_O	PCLK,SDRAM,BCLK		30		ohm

PACKAGE INFORMATION



48 PIN SSOP

ORDERING INFORMATION

For part ordering, please contact our Sales Department:

45437 Warm Springs Blvd., Fremont, CA 94539, USA

Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER

The order number for this device is a combination of the following: device number, package type and operating temperature range.

PLL52C62-01 X C

PART NUMBER

TEMPERATURE
C=COMMERCIAL
M=MILITARY
I=INDUSTRIAL

PACKAGE TYPE
X=SSOP