

AVX



AVX
Low Inductance Capacitors

Low Inductance Chip Capacitors



Introduction

As switching speeds increase and pulse rise times decrease the need to reduce inductance becomes a serious limitation for improved system performance. Even the decoupling capacitors, that act as a local energy source, can generate unacceptable voltage spikes: $V = L (di/dt)$. Thus, in high speed circuits, where di/dt can be quite large, the size of the voltage spike can only be reduced by reducing L .

Figure 1 displays the evolution of ceramic capacitor toward lower inductance designs over the last few years. AVX has been at the forefront in the design and manufacture of these newer more effective capacitors.

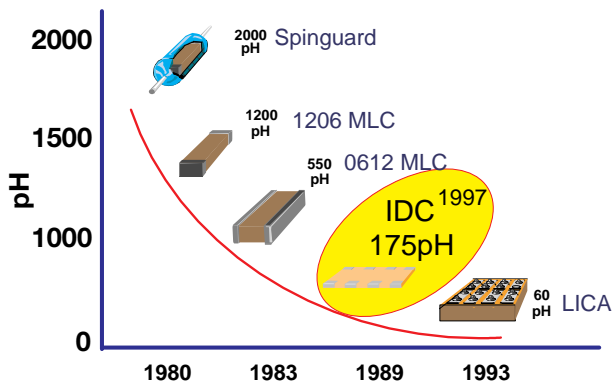


Figure 1. The evolution of Low Inductance Capacitors at AVX (values given for a 100 nF capacitor of each style)

LOW INDUCTANCE CHIP CAPACITORS

The total inductance of a chip capacitor is determined both by its length to width ratio and by the mutual inductance coupling between its electrodes. Thus a 1210 chip size has lower inductance than a 1206 chip. This design improvement is the basis of AVX's low inductance chip capacitors, Li Caps, where the electrodes are terminated on the long side of the chip instead of the short side. The 1206 becomes an 0612 as demonstrated in Figure 2. In the same manner, an 0805 becomes an 0508. This results in a reduction in inductance from 1200 pH for 0805 to only 600 pH for the 0508. Standard designs and performance of these Li Caps are given on pages 4 and 5.

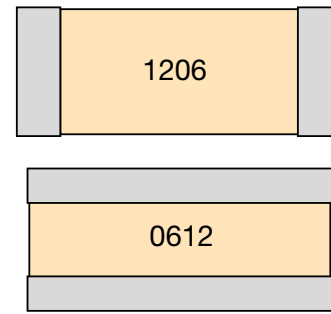


Figure 2. Change in aspect ratio: 1206 vs. 0612

LOW INDUCTANCE CHIP ARRAYS (LICA®)

Further reduction in inductance can be achieved by designing alternative current paths to minimize the mutual inductance factor of the electrodes (Figure 3). This is achieved by AVX's LICA® product which was the result of a joint development between AVX and IBM. As shown in Figure 4, the charging current flowing out of the positive plate returns in the opposite direction along adjacent negative plates. This minimizes the mutual inductance.

The very low inductance of the LICA capacitor stems from the short aspect ratio of the electrodes, the arrangement of the tabs so as to cancel inductance, and the vertical aspect of the electrodes to the mounting surface.

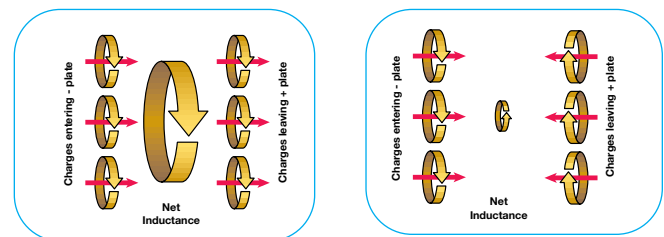


Figure 3. Net Inductance from design. In the standard Multilayer capacitor, the charge currents entering and leaving the capacitor create complementary flux fields, so the net inductance is greater. On the right, however, if the design permits the currents to be opposed, there is a net cancellation, and the inductance is much lower.

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Low Inductance Chip Capacitors



Low Inductance Chip Arrays (LICA®)

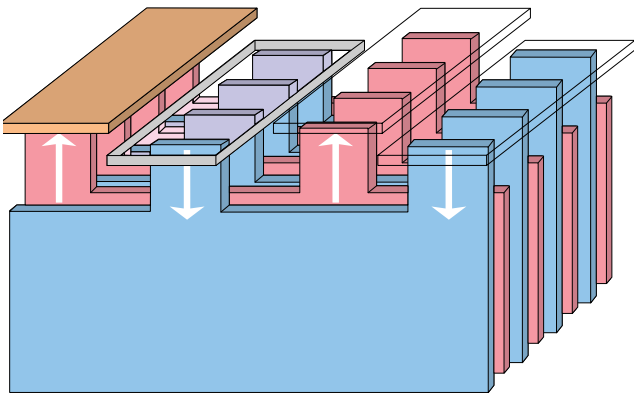


Figure 4. LICA's Electrode/Termination Construction. The current path is minimized – this reduces self-inductance. Current flowing out of the positive plate, returns in the opposite direction along the adjacent negative plate – this reduces the mutual inductance.

Also the effective current path length is minimized because the current does not have to travel the entire length of both electrodes to complete the circuit. This reduces the self inductance of the electrodes. The self inductance is also minimized by the fact that the charging current is supplied by both sets of terminals reducing the path length even further!

The inductance of this arrangement is less than 100 pH, causing the self-resonance to be above 50 MHz for the same popular 100 nF capacitance. Parts available in the LICA design are shown on pages 6 and 7.

Figure 5 compares the self resonant frequencies of various capacitor designs versus capacitance values. The approximate inductance of each style is also shown.

Active development continues on low inductance capacitors. C4 termination with low temperature solder is now available for plastic packages. Consult AVX for details.

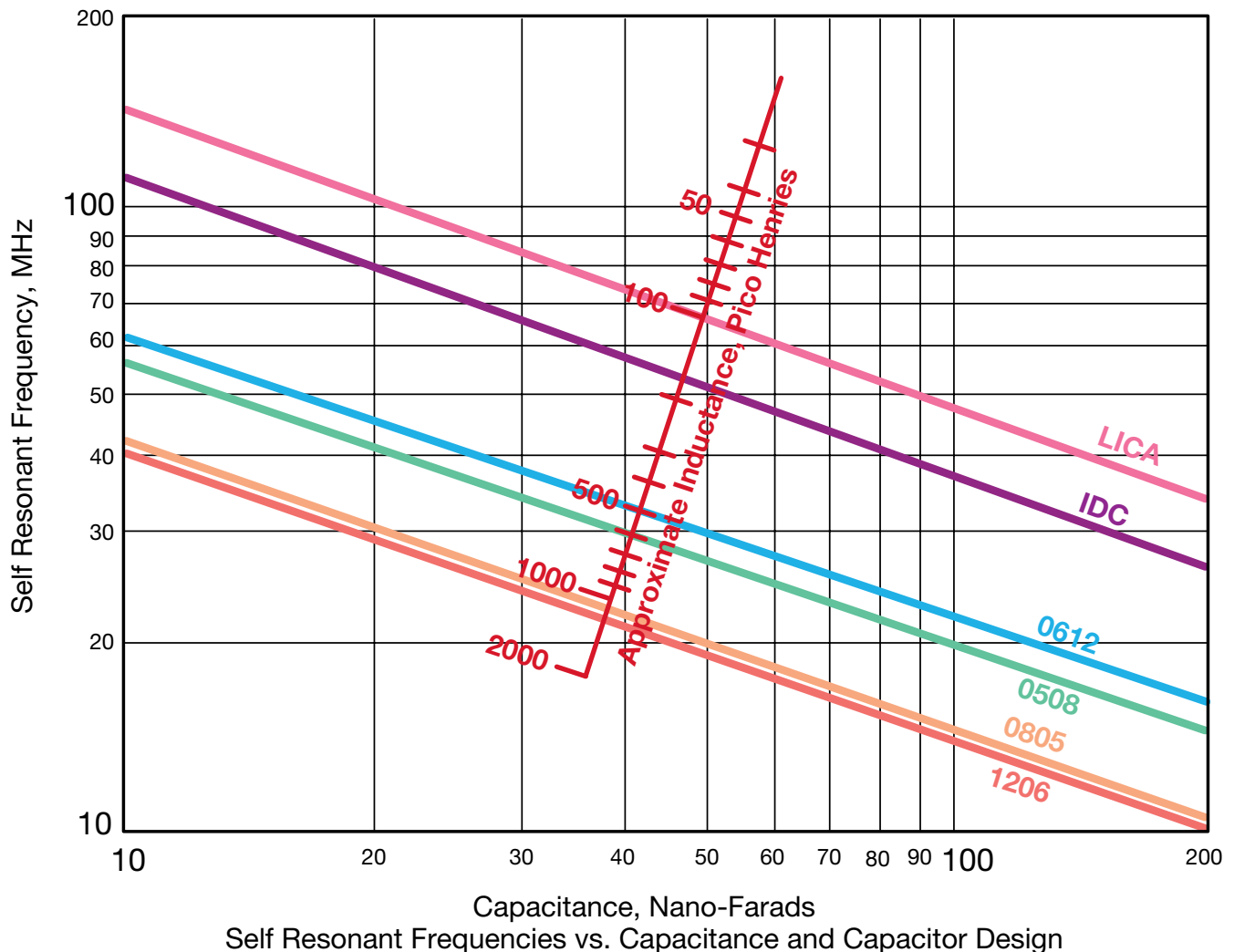


Figure 5.



Low Inductance Chip Capacitors

Specially Designed MLC Chips for Low Inductance



AVX's low inductance capacitors are designed for use in high speed circuits. Their aspect ratio and size have been optimized to reduce inductance from the 1 nH range found in normal chip capacitors to less than 0.4 nH. Their low profile is ideal for surface mounting or inside cavity mounting, adjacent to the IC itself.

HOW TO ORDER:

0508	5	C	822	M	A	T	1	W
AVX Style	Voltage	Temperature Coefficient	Capacitance Code	Capacitance Tolerance	Failure Rate	Termination	Marking Packaging	Special Code
0508 0612	50V = 5 25V = 3 16V = Y	C = X7R G = Y5V	(2 significant digits + no. of zeros) Examples: 10 pF = 100 100 pF = 101 1,000 pF = 102 22,000 pF = 223 220,000 pF = 224 1 μF = 105	M = ±20% Z = +80,-20% P = GMV K = ±10%	A = Does not apply H = High Rel*	T = NiGuard Nickel Barrier Solder Plate	9 = Bulk Unmarked 1 = Reel Unmarked	Thickness: mm (in.) U=.51 (.020) max V=.76 (.030) max. W=1.02 (.040) max.

*Consult factory for details.

CAPACITANCE RANGE: X7R AND Y5V DIELECTRIC

Dimensions: millimeters (inches)

AVX Style	0508	0612
Length (L)	MM (in.) 1.27 ± .25 (.050 ± .010)	1.6 ± .25 (.060 ± .010)
Width (W)	MM (in.) 2.0 ± .25 (.080 ± .010)	3.2 ± .25 (.126 ± .010)
Separation (X)	MM (in.) min. 0.38 (.015)	0.50 (.020)
Terminal (t)*	MM (in.) 0.50 max. / 0.13 min. (0.020 max. / 0.005 min.)	0.46 max. / 0.13 min. (0.018 max. / 0.005 min.)

MAXIMUM CAPACITANCE VALUES, (μF)

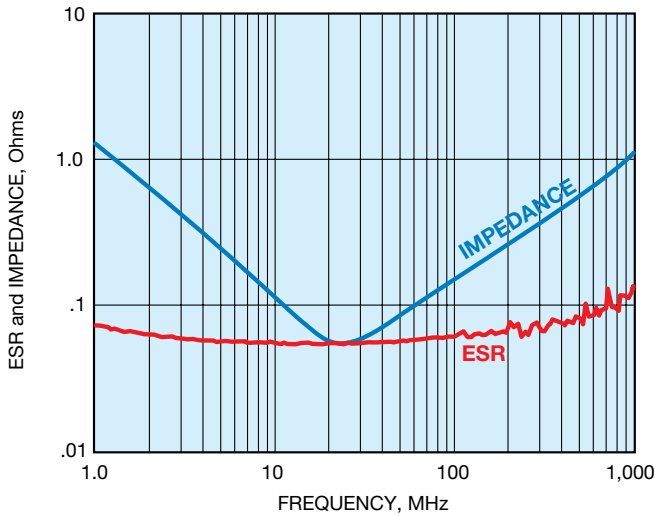
Thickness (T)	Size	X7R			Y5V		
		10V	16V	25V	10V	16V	25V
.050" MAX. THK.	0612	2.2	1.0	.27	6.8	3.3	1.2
	0508	.68	.27	.1	2.2	1.0	.47
.040" MAX. THK.	0612	1.5	.68	.22	4.7	1.8	.82
	0508	.47	.18	.056	1.5	.56	.22
.030" MAX. THK.	0612	1.0	.47	.12	3.3	1.5	.56
	0508	.47	.18	.056	1.5	.56	.22
.020" MAX. THK.	0612	0.47	.18	.056	1.5	.68	.27
	0508	0.22	.082	.022	0.68	.33	.12

Low Inductance Chip Capacitors

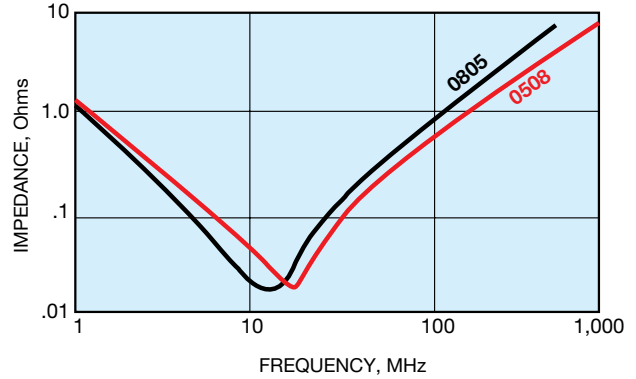
Specially Designed MLC Chips for Low Inductance



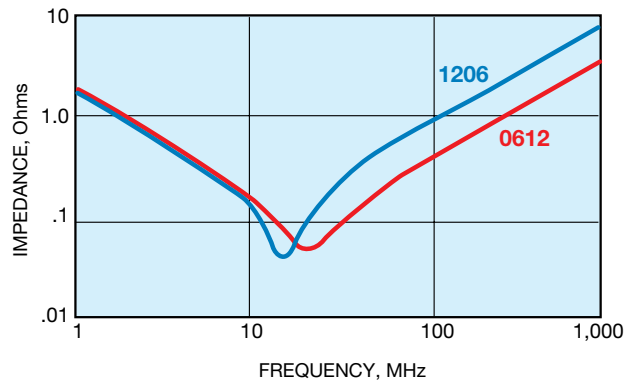
ESR and Impedance vs. Frequency
0612 0.1 μ F - X7R



Impedance vs. Frequency
0805 vs. 0508 0.1 μ F - Y5V



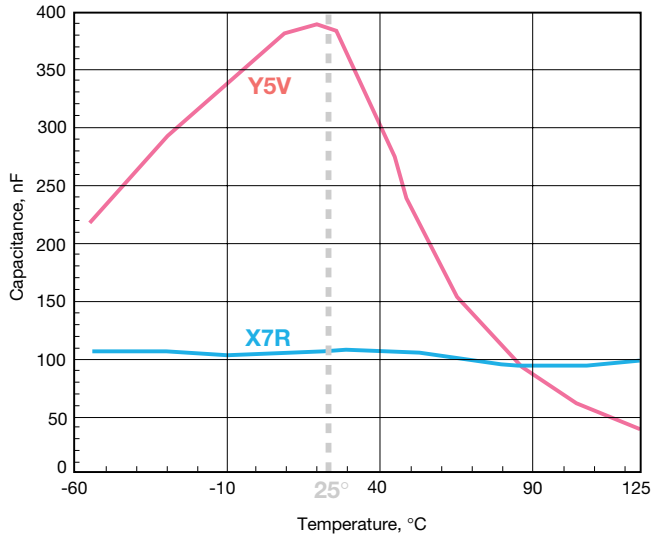
0612 vs. 1206



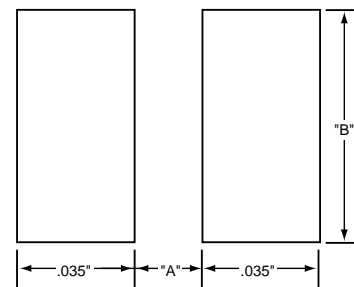
TYPICAL INDUCTANCE FOR 100nF CAPACITANCE

Chip Size	pH
0508	600
0612	500

Typical Capacitance vs. Temperature



RECOMMENDED SOLDER LANDS

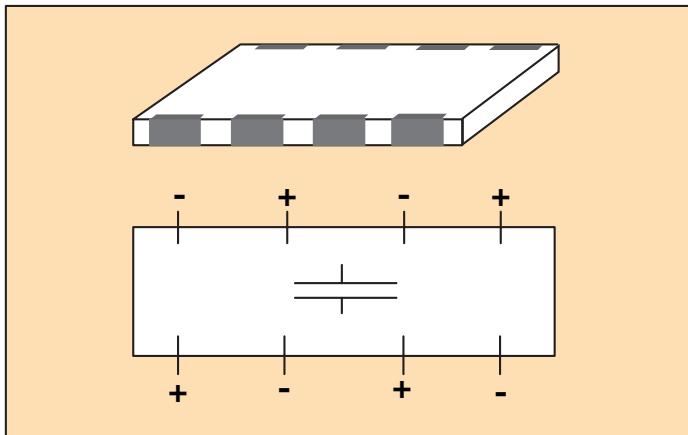


Chip Size	"A"	"B"
0508	.020"	.080"
0612	.030"	.120"

Low Inductance Chip Capacitors



InterDigitated Capacitor (IDC)



GENERAL DESCRIPTION

AVX's interdigitated capacitor is a very low inductance, surface mount capacitor. A measured inductance of 175pH makes this the lowest, FR4 mountable device in the industry. With the high speed microprocessors approaching 500MHz, and beyond, the need for low inductance, decoupling caps becomes critical. Also, by connecting the device with eight (8) vias to the power and ground planes, the inductance of the entire system can be lowered. This allows engineers to speed up board interconnect for the current, and next generation, of microprocessors.

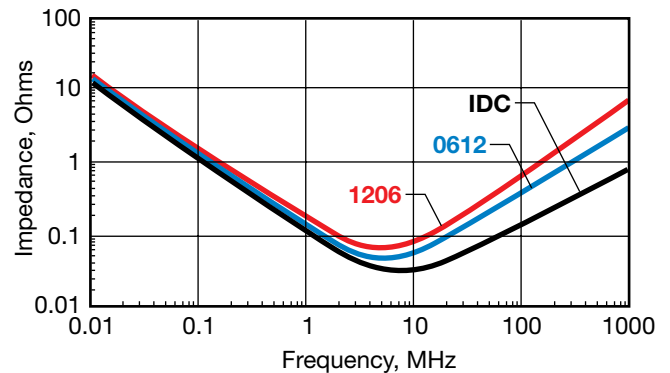
PART NUMBER

W	3	L	1	Y	C	105	M	A	T	3	A
Style	Size	Low Inductance	Number of Caps	Voltage Y=16V Z=10V 6=6.3V	Dielectric C=X7R	Capacitance Code	Tolerance M=±20%		Terminations T= Plated Ni and Solder	Packaging Code (Reel Size) 1=7" Reel Embossed Tape 3=13" Reel Embossed Tape	

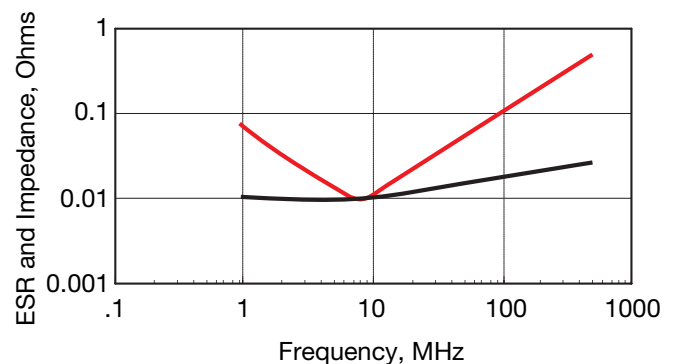
Package Style	Measured Inductance (pH)
IDC	175
0612	550
1206	1200

Capacitance (µF)		.047	0.1	0.22	0.47	0.68	1.0	2.2
X7R	16V							
	10V							
	6.3V							

Impedance Characteristics of 1µF - X7R



Typical Impedance and ESR - 2.2µF - ESR



PERFORMANCE CHARACTERISTICS

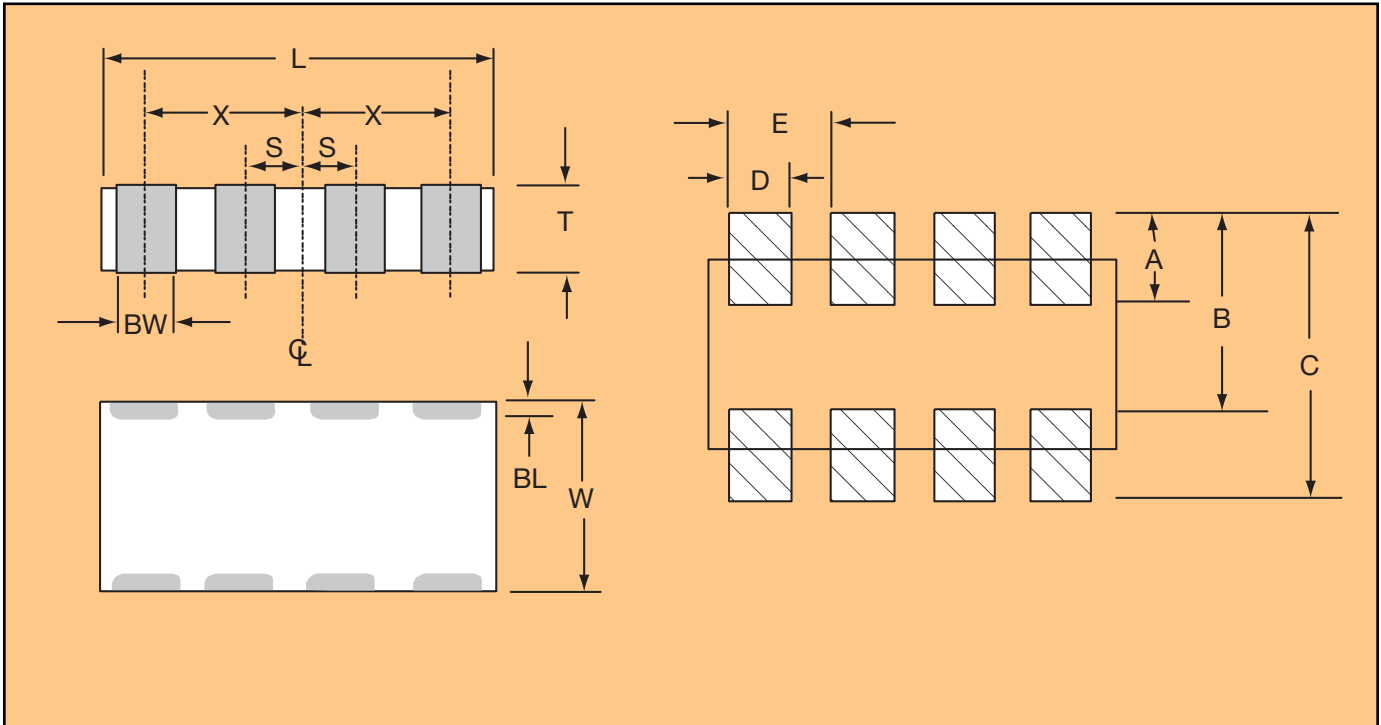
Capacitance Tolerance	X7R ±20%
Dissipation Factor	For 16 volts: 3.5% max. For 10 volts: 5% max. For 6.3 volts: 6.5% max.
Insulation Resistance (+25°C,VDC)	100,000MΩ min. or 1,000MΩ-µF min., whichever is less



Low Inductance Chip Capacitors



InterDigitated Capacitor (IDC)



PART DIMENSIONS

	L	W	T	BW	BL	P	X	S
Inches	.126±.008	.063±.008	.048 max.	.016±.004	.007	.030 ref	.045±.004	.015±.004
(mm)	(3.2±0.2)	(1.6±0.2)	(1.22 max.)	(0.41±0.1)	(0.18)	(0.76 ref)	(1.14±0.1)	(0.38±0.1)

PAD LAYOUT DIMENSIONS

A	B	C	D	E
.035	.065	.100	.018	.030
(0.89)	(1.65)	(2.54)	(0.46)	(0.79)

ASSEMBLY NOTES

AVX recommends a minimum spacing of 0.020" between parts when placing them end to end on assembly boards. The purpose of this spacing is to facilitate post assembly board cleaning and inaccuracies in pick and placement, due to machine placement tolerances.

Low Inductance Chip Capacitors



LICA® Low Inductance Decoupling Capacitor Arrays



LICA® arrays utilize up to four separate capacitor sections in one ceramic body (see Configurations and Capacitance Options). These designs exhibit a number of technical advancements:

Low-inductance features—

- Low resistance platinum electrodes in a low aspect ratio pattern
- Double electrode pickup and perpendicular current paths
- C4 “flip-chip” technology for minimal interconnect inductance

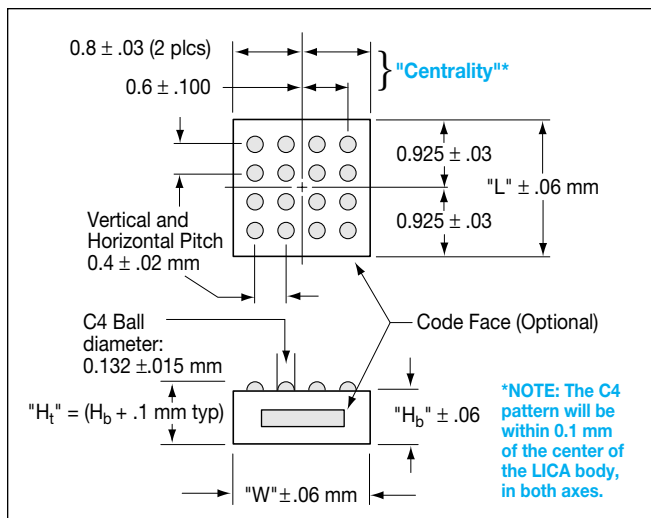
HOW TO ORDER

LICA	3	T	802	P	1	C	A	4
Style & Size	Voltage 25V = 3	Dielectric T = T60T	Cap/Section (EIA Code) 102 = 1000 pF 103 = 10 nF 104 = 0.1 mF	Capacitance Tolerance M = ±20% P = GMV	Height Code 1 = 0.875mm 3 = 0.650mm	Termination C = C4 Solder Balls-97/3 A = Thin-film O = Others D = Low Temp C4 Solder Balls	Reel Packaging M = 7" Reel R = 13" Reel 6 = 2"x2" Waffle Pack C = 4"x4" Waffle Pack U = Termination Side Up In 4"x4" Waffle Pack	# of Caps/Part 1 = one 2 = two 4 = four

TABLE 1

Typical Parameters	T60T	Units
Capacitance, 25°C	Co	Nanofarads
Capacitance, 60°C	1.4 x Co	Nanofarads
Capacitance, 85°C	Co	Nanofarads
Dissipation Factor 25°	8	Percent
DC Resistance	0.2	Ohms
IR, Minimum 25° (QUAD)	4.5	Gigaohms
Dielectric Breakdown, Min	500	Volts
Rated Voltage	25	Volts
Thermal Coefficient of Expansion	8.5	ppm/°C 25-100°
Inductance: (Design Dependent)	15 to 120	Pico-Henries
Use Frequency	DC to 1 Gigahertz	
Ambient Temp Range	-55° to 125°C	

C4 AND PAD DIMENSIONS



Code (Body Height)	Width (W)	Length (L)	Height Body (H _b)
1	1.600mm	1.850mm	0.875mm
3	1.600mm	1.850mm	0.650mm

TERMINATION OPTIONS

C4 SOLDER (97/3) BALLS



THIN FILM LANDS



Low Inductance Chip Capacitors



Typical Performance Curves

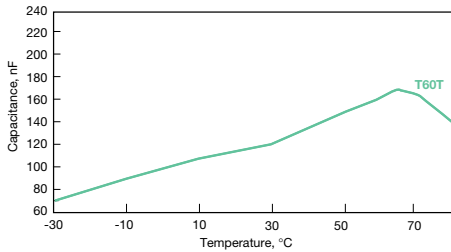


Figure 6 – Typical Temperature Characteristics of LICA® Dielectrics (Using 25V Single Capacitor)

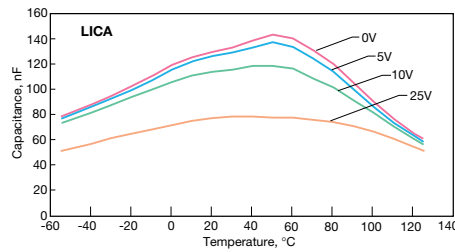


Figure 7 – Effect of Bias Voltage and Temperature on a 130 nF LICA® (T60T)

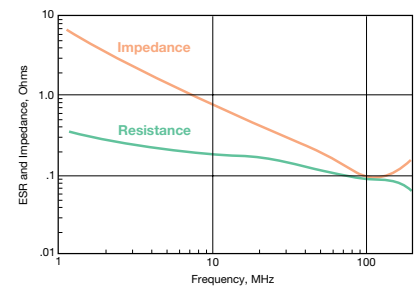


Figure 8 – Impedance vs. Frequency

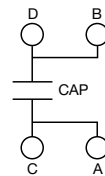
Configuration and Capacitance Options (Co)

SINGLE CAPACITOR DESIGN

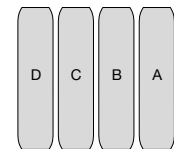
Typical nanofarads (nF) per section

Single 1 Cap/Unit	25V Rated		
	T60T	0.875	0.650
		130	90

Schematic



Code

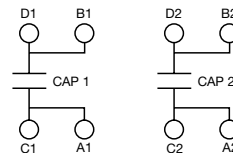


DOUBLE CAPACITOR DESIGN

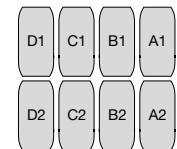
Typical nanofarads (nF) per section

Double 2 Caps/Unit	25V Rated		
	T60T	0.875	0.650
		60	40

Schematic



Code

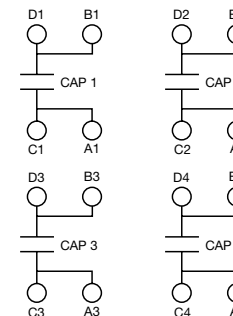


QUADRUPLE CAPACITOR DESIGN

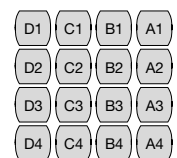
Typical nanofarads (nF) per section

Quad 4 Caps/Unit	25V Rated		
	T60T	0.875	0.650
		25	18

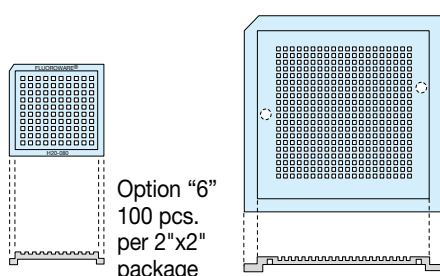
Schematic



Code



WAFFLE PACK OPTIONS FOR LICA®

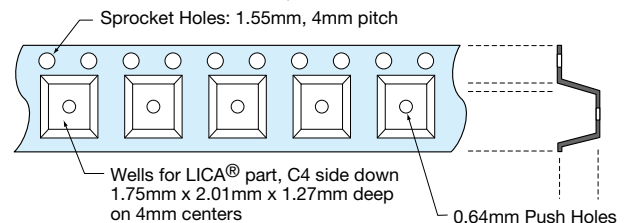


Option "6"
100 pcs.
per 2"x2"
package

Option "C" - Terminals down
Option "D" - Terminals up
400 pcs. per
4"x4" package

LICA® PACKAGING SCHEME "M" AND "R"

8mm conductive plastic tape on reel:
"M"=7" reel, "R"=13" reel





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FAX: 508-485-8471

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