TECHNICAL INFORMATION

ADVANCED DECOUPLING USING CERAMIC MLC CAPACITORS

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Abstract:

The ceramic multilayer capacitors were initially used for decoupling because of their low ESR and ESL compared to other styles of capacitors. Today, even these extreme low parasitics are unacceptable and new design techniques are being developed to obtain orders of magnitude reductions.

This paper will deal with the evolution of early methods to present uses and some future directions. It is intended to present a board awareness that might reduce repetition and may also introduce a possible solution to a problem.

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Introduction

The requirements for new methods of decoupling go hand-in-hand with developments in microprocessor and memory technologies. The faster speeds and greater densities dictate new constraints on energy transfer quantities and speed. This relationship is not totally exact. The density factor somewhat negates the size factor in that as trace size decreases allowing smaller energy requirements, the densities increase requiring more energy packets.

The ceramic multilayer capacitor (MLC) was first used in this instance because of its size, availability, density, performance, reliability, and cost. These units were the radial and axial leaded devices mounted on the PCB next to the power pin of the IC. The added inductance of the traces and the leads of the component were insignificant in the operation at the lower frequencies.

As a matter of fact, when these devices were being used for the early 16K and 64K DRAM decoupling, they were the best available with extremely low ESR and ESL. Today, these parasitics that were enviable back then are unacceptable now.

The recent developments in high speed decoupling have been in multiple simultaneous directions. The refinement of one design or technique has not necessarily led to the discovery of the next; but rather the developments in the different methods have usually been parallel, specific application dictated. It is the multiple specific requirements that have led to the varied venues in design and technology.

This paper will deal with the evolution of early methods to present uses and some future directions. It is intended to present a broad awareness that might reduce repetition and may also introduce a possible solution to a problem.

Decoupling Requirements

Decoupling is a means of overcoming physical and time constraints found usually in a digital circuit. Many times it is mistakenly referred to as filtering. These are two different applications and although a filtering circuit may perform decoupling, it is not optimally designed for that application. The same is true of a decoupling circuit. It may perform filtering, but it was not designed to perform this specific function in a prime manner.

Decoupling may be seen as a two terminal application and filtering as a three or four. Decoupling delivers energy to a specific point and filtering modifies a signal along a path.

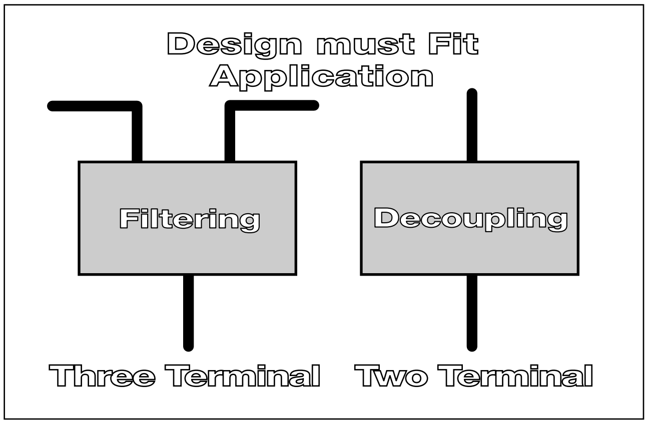


Figure 1. Type versus application.

The logic circuit may be seen as one of two possible states. On or off, true or false, high or low..., whatever logic interpretation is used, it is one of two states. The setting and detection of these levels is achieved with solid state switches that usually set and sense one state, and assume the other state is not set. There is a window of acceptance for this one state that is usually given as a percentage of the nominal. Moving near the minimum level creates some degree of uncertainty. There is a random determination of this signal as true or false. If a high frequency noise were then added to this set state, the degree of uncertainty increases as the level may move above and below the minimum required. The net effect is errors.

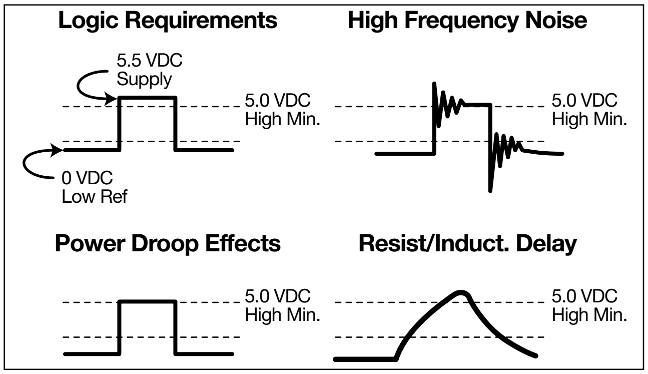


Figure 2. Logic requirements and error conditions.

The physical constraints of the circuit reduce the power supply's capability to deliver these quick bursts of energy at all locations equally. The resistance and inductance of the traces are the main parasitics in the early PCB layouts. The voltage apparent to the IC may be momentarily lower because of the time lag developed by the parasitics (*droop* or *Vdroop*) or it may be contaminated by voltages developed across the RLC circuit causing a ringing or high frequency AC noise to appear on the bus (sometimes referred to as *burst* or *Vburst*). The decoupling capacitor acts as a reservoir of energy located near the point of requirement. It delivers energy independent of the power supply during the quick burst period, with enough reservoir to maintain the required voltage level.

With the 16K and 64K DRAMs, there was a noticeable problem with error generation due to noise on the board. During refresh cycles, there was an instantaneous demand for energy by all ICs on the board. During access times, transients may be generated by simultaneous switching within the IC associated with multiple events such as address coding. As board population, memory size, and logic complexity increased, the total energy required also increased.

It was found that the layout of the board offered a great deal of inductance and resistance to this quick energy burst. It was decided to use a capacitor as a small reservoir of energy near each IC to offer the quick energy burst without delay. The capacitors would then recharge to the power supply voltage during the off time of the DRAM. An additional capacitor was placed at the power entry position of the board because this quick recharge request was generating a noise back to the power supply and to other boards on the power supply. The power entry capacitor must perform two duties: *filtering* and *decoupling*.

The ceramic MLC was used for the circuit level or individual IC decoupling (at least 0.01 µF) and the power entry capacitor was usually a tantalum or electrolytic (tens of µF). The MLC's performance and adaptability to the assembly process were its reasons for preference. The tantalum or electrolytic was usually soldered on afterward because there were few to a board, regardless of board density. The large value capacitors were used because they were supplying energy to all circuit level capacitors and had to be much larger than the sum of the circuit level capacitors. If there were problems in the initial testing of a new layout, more capacitors were randomly added until the problem disappeared.

As the use of the DRAM grew, so did the MLC. The rule of design was for every IC there had to be an accompanying MLC. With the development of the 256K and 1M DRAM, the rule remained the same.

Because there was a pattern established through the 256K DRAM that the larger the memory, the larger the capacitance, it was thought that as the size of the DRAM increased, so would the capacitance. The 1M DRAM refuted this as it required smaller energy for each element and the total capacitance remained the same as the 256K. This economizing should continue into the 4M DRAM and beyond as densities increase with smaller trace size and the energy required for each element decreases.

Capacitance Make-up

A capacitor consists of two conductive plates separated by an insulative material capable of storing electrical charge for later release. Its rating of capacitance is determined by the amount of charge for a given voltage. The MLC is a sandwich of alternating dielectric and plates, with successive plates terminated at opposite edges.

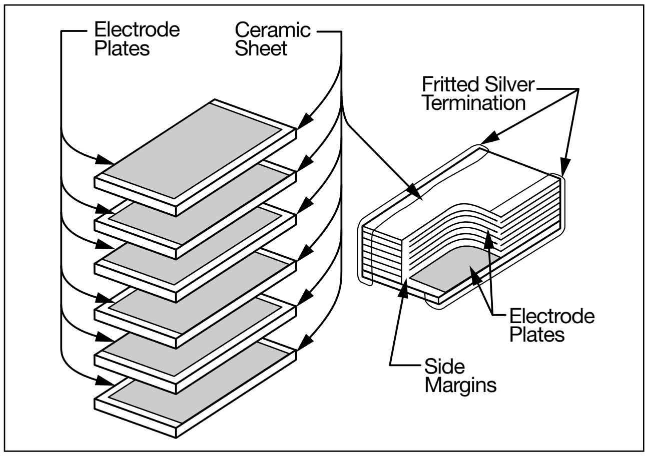


Figure 3. Ceramic multilayer construction.

The ideal capacitor has no losses in its conductive plates and dielectrics. The real world gives us lousy conductors and dielectrics. There is a current path defined by the plates and, because of this, there is an element of inductance associated with the plate configuration. Also, because one plate is charging while its adjacent counterpart is discharging, there is a mutual coupling factor adding to the inductance.

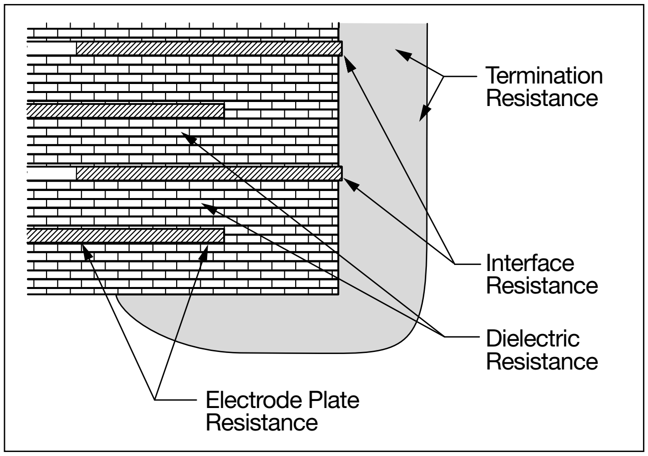


Figure 4. ESR distribution in MLC capacitor.

Effective Series Resistance (ESR) is a term referring to the resistive losses in a capacitor. For the MLC, this loss consists of the distributed plate resistance of the metal electrodes, the contact resistance where the internal electrode and external termination meet, and the dielectric resistance (Figure 4). There is an additional resistance of the termination metal to the height of each electrode above the board which must also be accounted for else an infinitely high capacitor would have 0 ESR.

The Effective Series Inductance (ESL) defines that loss element which must be overcome as current flow is constricted within a given envelope. The tighter the restriction (High Aspect Ratio or L/W), the higher the ESL and vice versa. It is almost the same as a ribbon conductor with the inductance calculation as follows:

$$L_{(nH)} = 5 \times [\ell n \{(2 \times \text{length}) / (B + C)\} + \tfrac{1}{2}]$$

where length = length in inches

B + C = cross sectional area dimensions

This formula is not exact in that the plates are not isolated and there is some mutual coupling, but this formula does point out the relationship that exists to a large degree in the plate design.

Early Leaded MLCs

In the initial decoupling scheme, radial and axial leaded MLCs were used because they conformed to the state-of-the-art. The additional lead inductance of 1 to 3 nH was insignificant when considering that the entire path to the IC represents 24 nH total. This inductance was allowable at 1 mHz to 4 mHz and becomes prohibitive at 8 mHz to 12 mHz and beyond. This inductance of the chip itself can range from 1 nH to 2 nH.

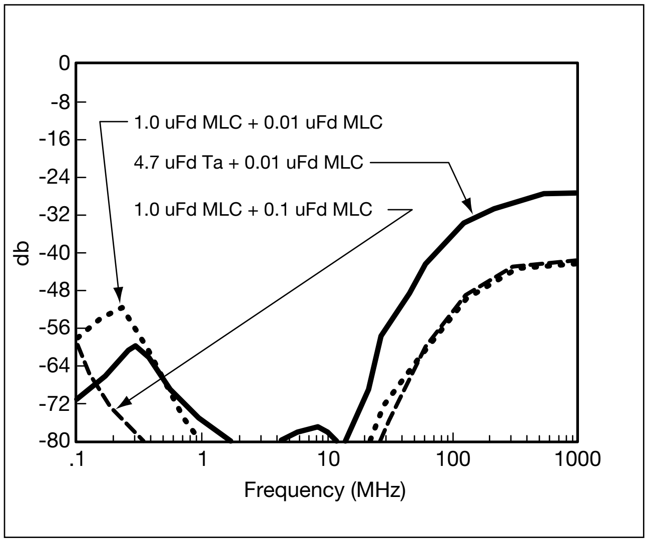


Figure 5. Noise transfer function from switched gates to power entry point.

The inductance of the radial leaded device is lower than the axial, but because most insertion equipment could better handle the axial, the axial dominated the application.

With the chart shown in Figure 5, some variations of the basic decoupling scheme were attempted. The initial setup used a 0.01 µF MLC at each IC (circuit level decoupling capacitor) and a 10 µF tantalum for power entry (board level or power entry decoupling capacitor). The chart reflects the average noise generated on a memory board with the previous setup. Also shown is the result of replacing the 4.7 µF tantalum with a 1.0 µF MLC. The high frequency noise has decreased by 15 to 20 dB, but the low frequency noise has increased. In order to improve the low frequency noise problem, the circuit level decoupling capacitors were increased to 0.1 µF and the resulting low frequency noise level is now below the initial setup.

Ceramic vs. Others

There is characteristic behavior depending on the type of capacitor used. The following chart (Figure 6) depicts type of capacitor behavior response to a current pulse that changes from 0 amperes to 200 milliamperes in one second, and then maintains the 200 mA as a constant current source. This di/dt generates a series of voltages corresponding to the capacitive, resistive, and inductive elements of the device tested. I won't go into detail here how these elements can be deduced for the resulting voltages, but I must point out that after the transition, the device is in a constant current mode and should exhibit a constantly rising voltage after the pulse voltage, generated in the transition period, dies out.

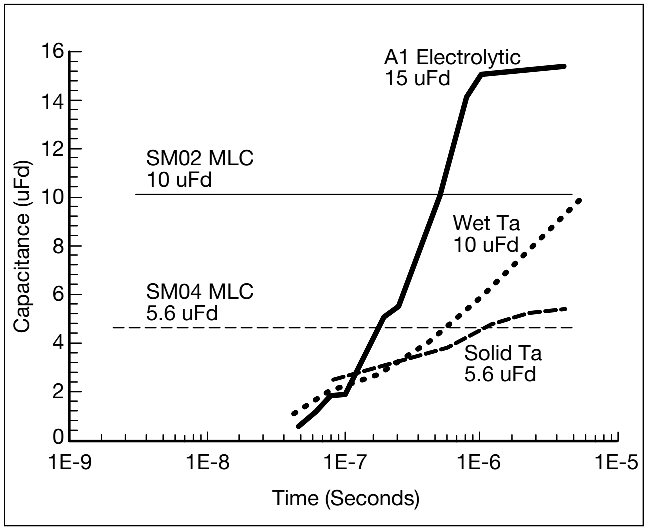


Figure 6. Capacitance as a function of dv/dt slope.

The time that it takes the initial pulse voltage to die out depends upon the internal and external impedance loop. For the tantalum and electrolytics, this time was in excess of 40 nS. The aftereffect for these types also shows that the dv/dt slope which should be constant is instead very steep at the beginning and decaying to a constant only after milliseconds, or tens of milliseconds have passed. This means that in the early portion of the pulse, the capacitor behaves as one of 1/10 to 1/100 of the marked value. This type of capacitor cannot perform well in higher frequencies. This is also borne out in the earlier chart depicting noise generated on a memory board. It has enough capability to assist low frequency reduction, but it cannot respond to high frequency. As a matter of fact, if this capacitor remains in a circuit beyond its capabilities, the capacitor itself then becomes an additional source of noise generation.

What is the capability of the MLC? The axial and radial can get down to 2 nH of inductance. The surface mount chips can achieve nearly 1 nH. Our measurement of capacitance using the current surge method shows the ESL pulse dying out in as little as 1 nS after steady state current is achieved for the chips. That they exhibit any inductive pulse does point out that the standard MLC does have some vulnerability — there is no perfect capacitor!

The Beginning of Improved Decoupling Schemes

The first step to improve decoupling involved the surface mount MLC chips. First there was the chip mounted to the PCB. This was basically a low profile 1210 (120 mils length, 100 mils width) chip, surface mounted beneath the IC on the PCB. This eliminated the loop circuit trace required to bring ground and power to the solder pads of the chip. This alone eliminated 9 to 12 nH of inductance. This technique did use up most of the real estate beneath the IC.

This chip was then proposed as an internal decoupling capacitor mounted on the IC leadframe and molded in the package. This chip was capable of 1.2 to 1.9 nH depending upon capacitance. The reluctance to use this device was borne of adding another component to the IC that would effect reliability of the package, which was the responsibility of the IC manufacturer.

Multiple power plane PCBs also greatly reduced the inductance to the solder pads and allowed placement of the chip at a perimeter location not restricted to beneath the IC.

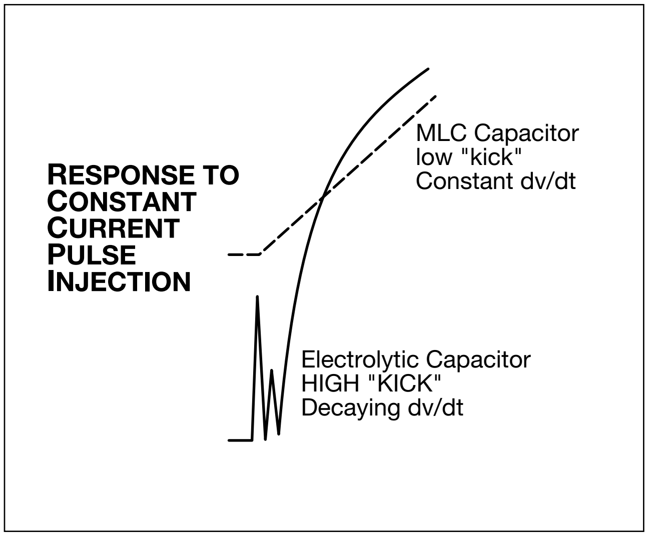


Figure 7. Comparative response of MLC and Ta or electrolytic capacitor.

Co-existing Low Profile Decoupling Capacitors

An arrangement was made utilizing a single layer of film sandwiched between two plates, such that extending out from the perimeter of the sandwich, “pins” were formed form the metal plates. These pins were then bent in a common direction perpendicular to the plane. These pins would then *co-exist* in the socket with the IC pins. Although this is how the majority of these devices were used, some soldered them to hole locations formed in the board.

The film was soon replaced with a single layer ceramic to increase the capacitance. This device could be formed to contact any pin arrangement within the center perimeter with 2 to 16 pin arrangements normal. Because the inductance was mostly in the pin extension from the plate, they could easily fit the DIL arrangements without adding significant inductance.

In leaving the spread out designs of the DIL arrangement, a matrix or array of pin connections was utilized in order to increase the circuit density involved with the IC. For the most part, the power and ground connections were placed near the empty square found in the center.

The PGA required that the coupling capacitor be located near the center of the device, close to the pins transferring power into the device.

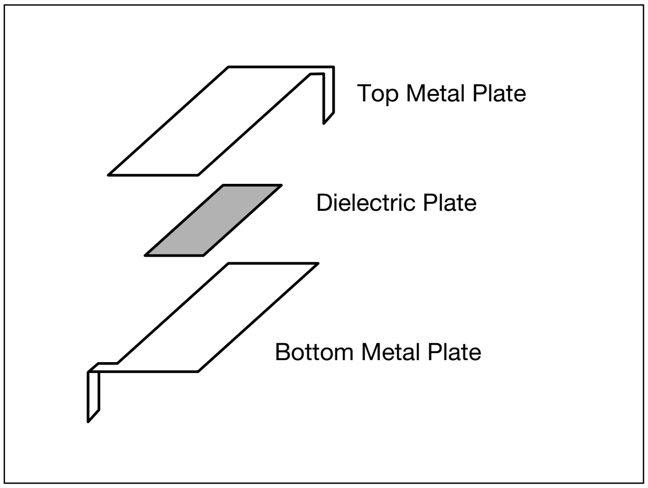


Figure 8. Co-existing decoupling capacitor assembly.

The single layer ceramic offered little to the total inductance of this package, most of the inductance came from the physically determined current restriction of the pin and plate.

We tried the multilayer techniques with this approach because some of the PGA manufacturers were looking for larger capacitance values than the single layer and the mechanical fragility of the existing structure. The overall inductance was, again, dominated by the pin arrangement and stayed between 1.2 and 1.4 nH. We could easily achieve 1 to 5 µF in the eight pin PGA decoupling device, but the cost was considerably more than the existing device.

I should also point out that the capacitance of 0.2 µF for the single layer device was achieved using a Z5U or Y5E ceramic. These ceramics are extremely sensitive to heat and if the IC were to get to 60°C, the capacitance could lose as much as 30 or 40% of its original value. The 1 to 5 µF multilayer version of this device was built using X7R material, which would have dropped only 5 to 7% of its value at this temperature.

Sub NanoHenry Requirements

With the multiple power plane PCBs and substrates, and mounting the capacitor near the IC, total inductances approaching 2 nH were now achievable. The capacitor was no longer a small contributor to the overall inductance. With this realization, now we get a request for a capacitor with an ESL in the range of 700-800 pH.

IC circuit densities are going up further with trace sizes of 1 micron and below. It is no longer the refresh current burst only that has an enormous appetite for large, quick bursts of energy. The complexity is such that merely changing states of a large block of elements within the IC requires a large enough energy transfer that there is prohibitive noise burst generated when using an external decoupling capacitor. With the PGA devices, this is aggravated by the fact that the pin densities won’t allow near location (for all pins) of an external capacitor.

It was found that the ideal shape of a capacitor mounted within the IC near the die or within the PGA pin pattern was an 0805 (80 mils long, 50 mils wide) with a thickness ≦20 mils. The standard 0805 chip has an ESL in the range of 1.3 to 1.9 nH, depending upon capacitance value. What we learned with a previous product led us to redesign the part as an 0508 (50 mils long, 80 mils wide).

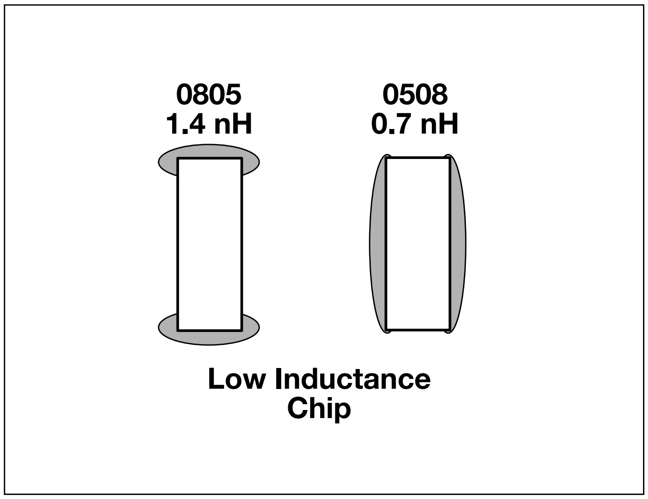


Figure 9. Sub nanoHenry MLC.

Again, the ESL of any device is a figure of how narrow and over what distance the current is restricted. The inductance of a plate is directly proportional to the length and inversely proportional to the width. Many times the ratio of length to width is expressed as aspect ratio. We reduced the aspect ratio from 1.6 to 0.625. The ESL for this particular 10,000 pF capacitor went from 1.4 nH to 0.75 nH.

The accompanying chart (Figure 10) depicts response to the constant current injection. If we were to assume that the voltage at transition time (1 nS) were attributable solely to ESL, you can readily see the reduction in noise generated during turn-on of this device.

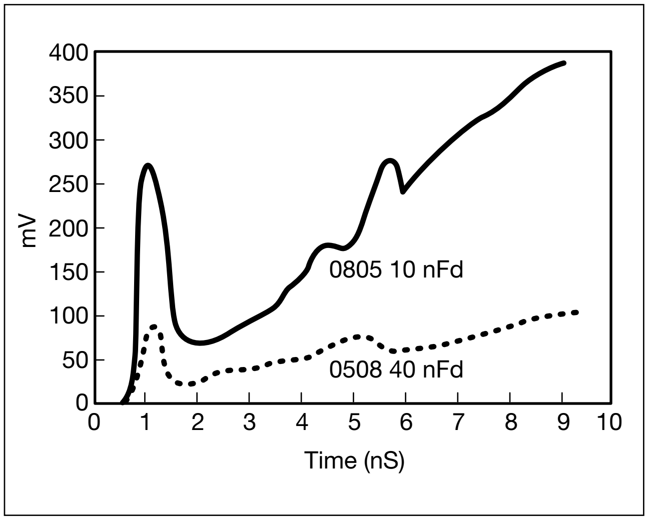


Figure 10. Voltage response to 200 mA/1 nS current pulse.

Decoupling Array

At the same time we were working on this product, we were requested to suggest some way of reducing the noise generation within a test head for a semiconductor manufacturer. They presented us with the fact that their yields on the die tests were enormously low and that they felt that the yield should have been much better.

The test head was typical in that it consisted of a multiple pin probe for the PGA carrier with capacitors tied across many of the traces leading to the pins for decoupling. We suggested that we design an array that would allow the pins to be fit within it, and the array would carry the ground, and power interconnects internally and the capacitance would be distributed throughout the array and presented at the base of the IC. They also had us put load capacitors in certain locations to optimize load capacitance matching.

The array is a monolithic structure resembling a large plate and multiple holes located at various locations. The pattern of the plates can be such that they afford singular capacitors to each hole or can be extended to allow multiple interconnect within the structure. It is an extension of the MLC technology that requires exact processing to maintain true location of the holes and minimal warpage in a fairly large surface area. It was earlier introduced as an EMI/RFI solution to filtering multiple signal lines as in a cable connector assembly.

The following sketch (Figure 11) depicts a typical arrangement. Also shown is the plate design involved in the ground and power plane plates. No hole should exist at an edge of a pattern but should be surrounded by plate area that will allow multiple direction of charge.

This surround technique is the same as with a discoidal capacitor. Because it has multiple direction current paths, there is little mutual coupling of charge related magnetic fields as with a parallel flow. There is even some cancellation as I will discuss later.

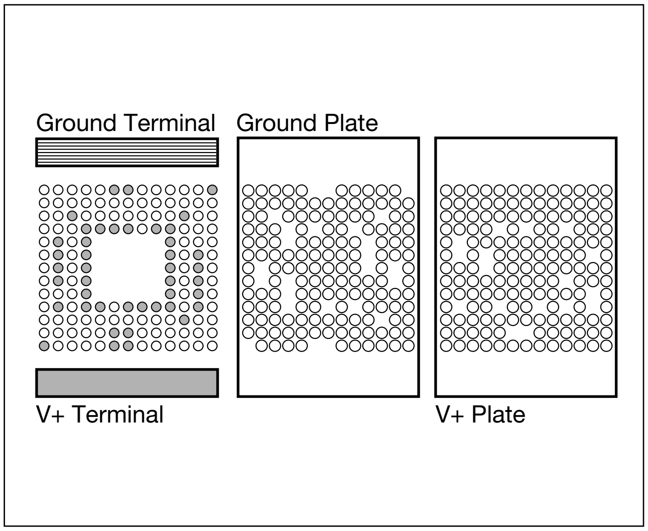


Figure 11. PGA decoupling pin arrangement.

The proof of the fix was in the enormous increase in yield achieved with this array approach. It was even discovered that the IC possessed an inherent flaw in the design where the inductance was measurable as a response from the IC during testing. This led to a revision of the design for the subsequent release of its successor.

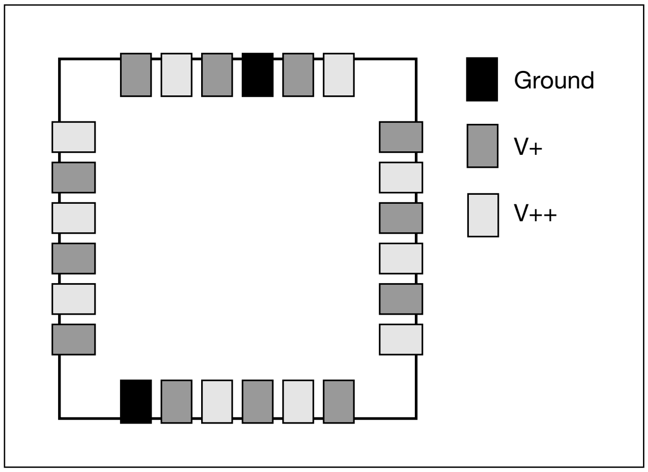


Figure 12. Decoupling cover array — 1" to ½" square.

A variation of the PGA array as shown in Figure 12 required the contacts to be made on the perimeter of the capacitor array. By using a bondable metal termination, this array would fit over the top of the IC die, extending over a cavity. Contact was with a wire bond between each contact along the edge of the capacitor array to a land area on the base substrate. We could easily add multiple power planes to the single device. We could not effectively test the ESL of this device and duplicate the application. Our customer did report that based on the voltage pulse recorded during test, the ESL of this device was in the neighborhood of 40 pH.

200 picoHenries (pH) ESL Requirement

We were also concerned about the larger power entry capacitor application. There were suggestions of putting ferrite beads or slowing down clock frequencies on memory boards because of so much noise passed back to the power supply. If this device were optimized for filtering to the extent that ferrite materials are required, its capability for decoupling would suffer dramatically. We believed that if a large ceramic capacitor were designed with a low enough ESL, this singular device could afford both the required filtering as well as achieve some decent decoupling.

At first we attempted to push the aspect ratio further. Specifically, a customer was requesting that we design a capacitor for decoupling his power plane at distributed locations on his board. He was specifically looking for a 5 µF capacitor with a resonance above 5 mHz. This equates to an ESL of less than 200 pH.

We designed a device with an aspect ratio of 0.2. When we measured the response, it showed us a resonant point of 3 mHz. This resulted in an ESL of ~550 nH. Hardly much of an improvement over the 750 nH for the 0508 with an aspect ratio of 0.625.

We realized that the common MLC technology approach would not work. Because charge concentration is densest at the internal corners opposite the termination edge, the majority of current carrying this charge would also occur near the outside edges. Although the current densities do decrease with lower aspect ratios, they do not decrease at the same rates as moving from aspect ratios of 5 to 0.5.

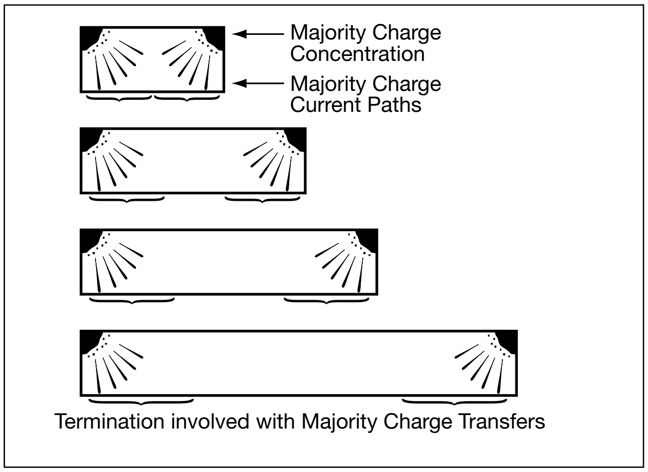


Figure 13. Aspect ratio limitations.

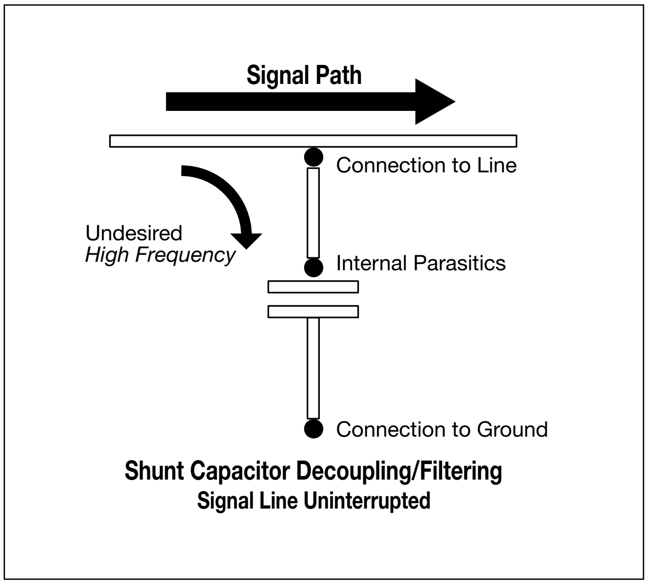


Figure 14. Typical filtering via shunt capacitance with three nodes of impedance.

There is the additional consideration in that the mutual coupling factor is still in existence as the opposite charged plate is located at a dielectric's thickness away. Though these plates are oppositely charged, the electron flow is in a common general direction.

In this mainly filtering application, we analyzed the component as a two terminal device (Figure 14) with main nodes of impedance that prohibit the high frequency flow: connection to line, internal parasitics, and connection to ground. What we wanted to do was eliminate the impedance node at connection to line or signal trace. We attempted to do this by intercepting the line and making that node an extension of the signal path and not the high frequency. The added impedance to the signal path was insignificant, and its removal from the high frequency noise path could only prove beneficial (Figure 15).

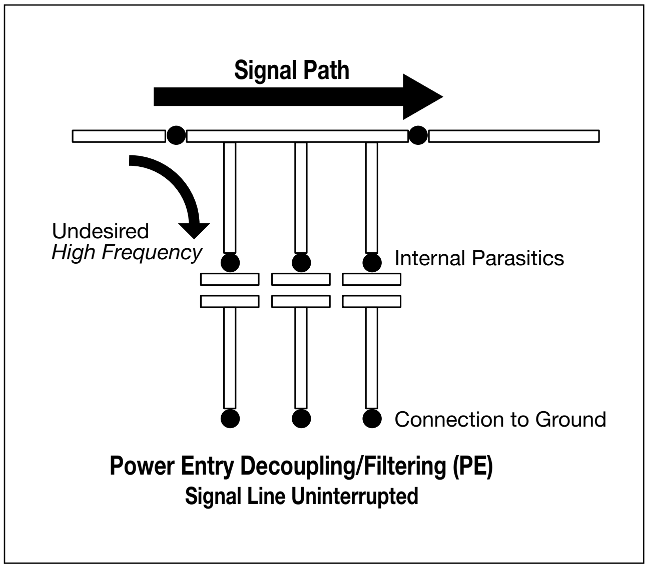


Figure 15. Three terminal or series attached shunt filter.

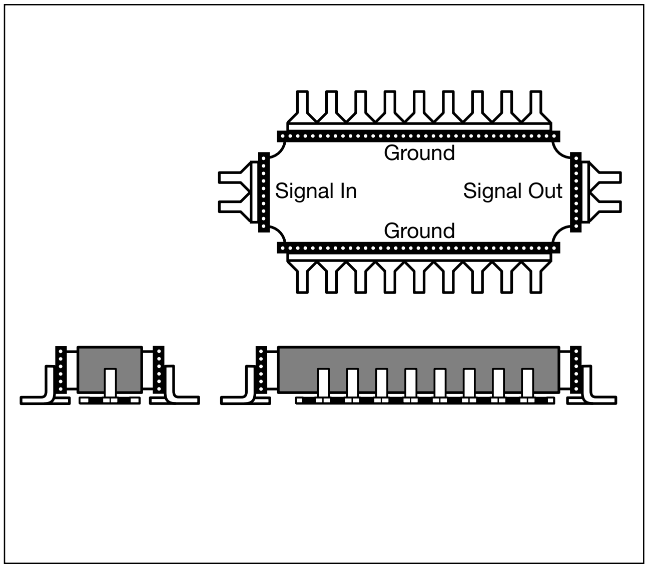


Figure 16. Power Entry (PE) three/four terminal filter.

Four Terminal Power Entry Capacitor

The result was a three or four terminal device with a signal plate feeding the signal through the monolithic structure, and a ground plate capacitively coupled to the signal plate via the dielectric. It contained signal input and output terminations at opposite edges, and two ground terminations at opposite terminations at a 90 degree axis displacement from the signal terminations.

At first, I was not impressed with comparison of the insertion loss of this device compared to standard MLCs or even alternate types. That is, until I fully analyzed what the results meant. A large change in inductance does not relate to a large change in resonance.

The chart of insertion loss versus frequency (Figure 17) shows a slight change in magnitude and frequency of maximum attenuation. When this data is analyzed, it reveals that the ESL is in the range of 128 pH. The ESR is 4.4 milliohms — not bad for a 2.2 µF capacitor.

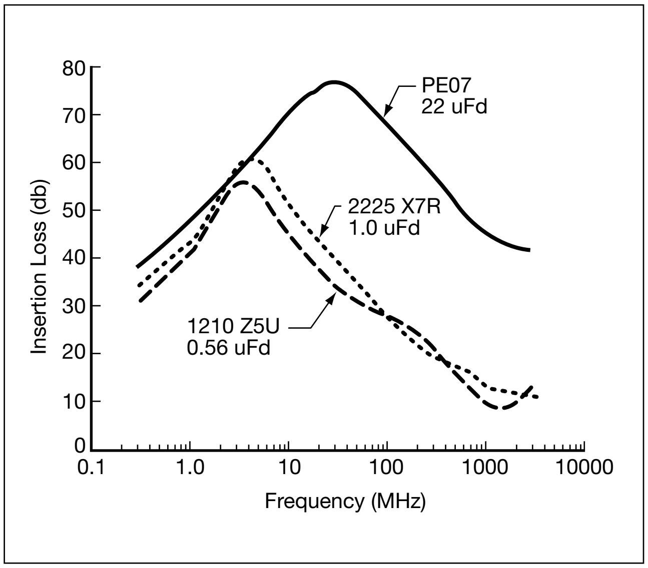


Figure 17. Insertion loss of Power Entry (PE) device and others.

When we tried to explain that this performance change was the result of the elimination of the one impedance node, we couldn't even convince ourselves. What is really going on is inductive cancellation. As the diagram depicts, the signal is center fed and the high frequency current paths to ground are in opposite directions. Because currents moving in the same direction reinforce each other's magnetic field, so do currents moving in opposite directions cancel each other's field.

The aspect ratio of the signal path was kept at unity or greater to help induce some impedance to the signal line, and the ground path aspect ratio was kept as low as possible to minimize the internal parasitics. This added benefits in that the device now resembled a distributed LRC low pass filter with distributed connections to ground—reducing the other two nodes of high frequency noise impedance.

I've digressed from my topic slightly in that the last device is more of a filter than a decoupling capacitor; but I need to introduce the development of the inductive cancellation techniques for the next product.

Power Plane Decoupling Capacitor

To effectively decouple, there is no benefit in defining the aspect ratios of the ground electrodes or power electrodes to be anything but unity. Reducing the ESL for either plane increases the ESL for the other plane. Also, since the device must condition two places in circuit board, why place DIP leads extending perpendicular from the capacitor to appropriate planes.

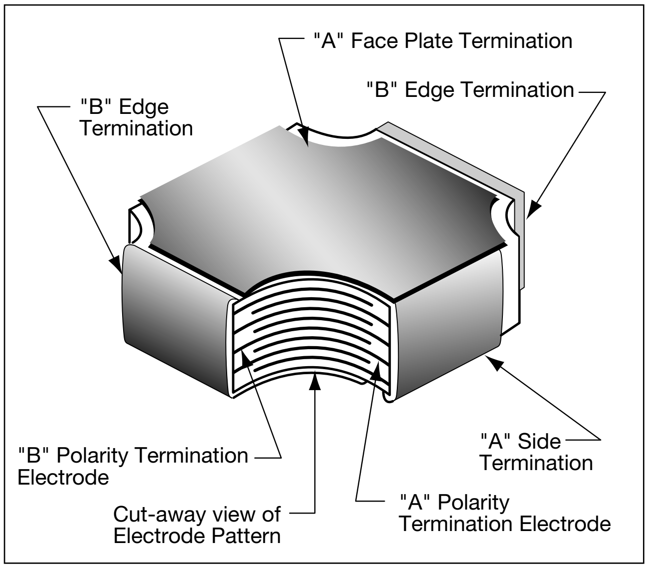


Figure 18. Construction of power plane decoupling capacitor (PPDCPL).

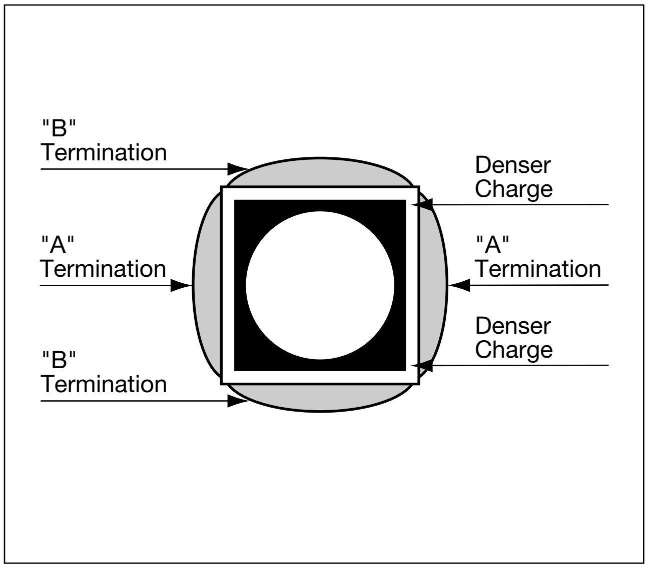


Figure 19. Majority charge distribution for PPDCPL.

The first attempt was in designing a 0.25" x 0.25" capacitor with four equally spaced terminations at each edge. We drilled the mother pad at the corner locations to facilitate the termination of these edges, We also tied the common terminations together with a band of silver termination that covered the larger faces of the unit. This was done for two reasons: to allow an electrical extension of the plane geometry, and to allow broad area contact between the plane and the capacitor.

There is an additional benefit in keeping the aspect ratio near unity: the charge distribution is equally divided along all edges with some charge concentration near the termination edges themselves — thus the charge movement is kept extremely short within the capacitor, enhancing ESL and ESR. The measured ESL of this device was in the range of 100 pH. I believe that it is much closer to 20 pH, but I have not attempted full perimeter contact of the termination face. Our attempts

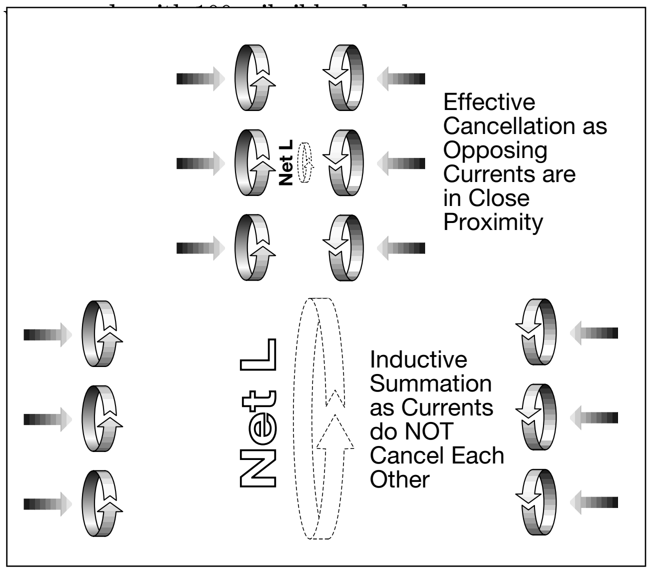


Figure 20. Loss of cancellation effects with large separation.

This design has its limitations. If the points of current injection are moved far enough apart, the cancellation effect is lost because they cannot react with each other as distance increases. We have established that this interaction occurs readily with singular chips less than 0.3" square.

The 10 µF 20 picoHenries (pH) Capacitor

Again, as with most of our applications, it was a customer's query that led to the next design. They needed a 10 µF capacitor, less than 100 mil thick, that would not resonate below 10 mHz.

If we took the approach of the last device, the capacitor would be nearly 1" square. This would cause us to lose our cancellation effects and the ESL would go up to about 500 pH.

What we did instead was to again use a modification of our array technology. We would make a 1" square device and inject the currents at rows that were ~0.25" apart on one side for one termination, and inject the currents at columns that were ~0.25" apart to the alternate internal plates from the opposite face for the other termination.

The diagram (Figure 21) might best describe this element. The rows and columns are segmented to allow equal terminations. The terminations are blind vias — the depth of the via is less than the thickness of the part and the bottom thickness affords electrical isolation of the two terminations.

The placement of this device as with the previous requires planning. Ideally, they fit in a window cut in the board. The termination for our testing was with soldered ribbon to the face terminations; sometimes singular ribbon extending beyond the perimeter of the part to the board, and sometimes multiple contacts along the perimeter on both sides of the device and board. With the 10 µF unit, I also used brass shimstock to form a frame overlapping the outside edge of the unit and the inside edge of the board, along the full perimeter. I used a conductive epoxy to mount the frame.

The response for the multiple ribbon shows a resonance of ~11 mHz, which correlates to ~20 pH of ESL. The full frame moved the resonance point up to ~13 mHz with an ESL of ~15 pH.

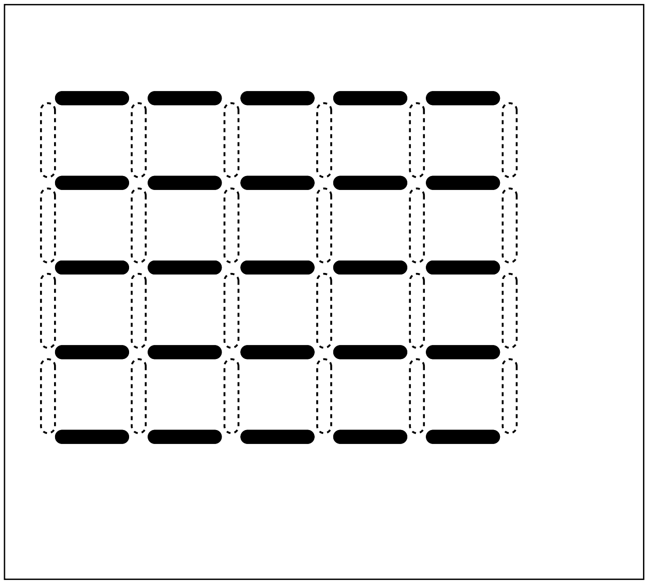


Figure 21. Large PPDCPL capacitor (1" square).

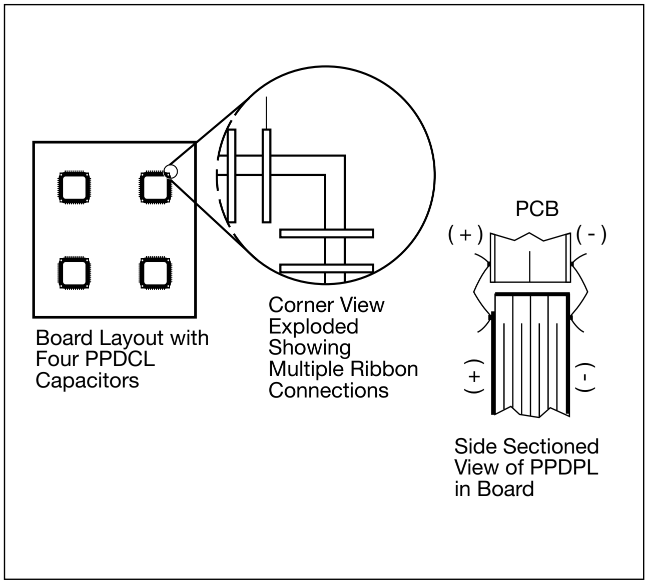


Figure 22. Window connection of PPDCPL.

Interdigitated Leads

This is an arrangement of the pins in a larger capacitor such that the adjacent pins are of opposite polarity (Figure 23). This eliminates the majority charge movement to adjacent corners opposite the termination edge in the standard MLC. Because it is being fed from both edges simultaneously, the majority charge concentration will be more equally divided over the effective area of the plate. This allows shorter current paths reducing both ESL and ESR.

The only inequality of charge distribution in this device is generated in a non-unity aspect ratio. This may be an enhancement if the aspect ratio is such as to cause the majority charge distribution to take place at the edges, along the terminating pins (>1). This may be offset by the fact that this aspect ratio also requires less area for termination (one of the nodes of ESR occurs at the termination to internal electrode interface).

The best pin arrangement for the interdigitated leaded capacitor utilizes the DIP or DIL arrangement. The SIP arrangement, especially for larger ceramics, leaves these large ceramic devices in a mechanically unsound mount.

This device is ideally suited for mounting on a surface where both ground and power traces can be laid out. It is an ideal decoupling capacitor because it delivers its energy in a two terminal node.

This method can also be applied to a circular shaped unit (Figure 24) where the majority charge distribution is almost perfectly equal throughout the perimeter. This effect equally divides the current flow among all pins and allows for an extremely short path for charge movement.

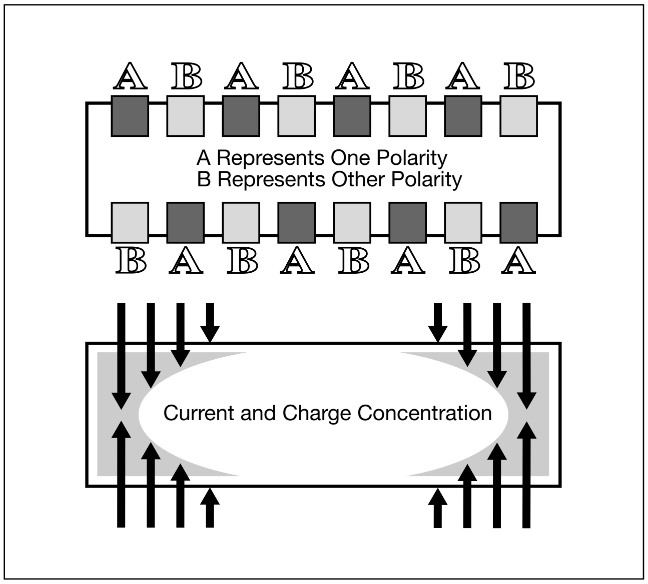
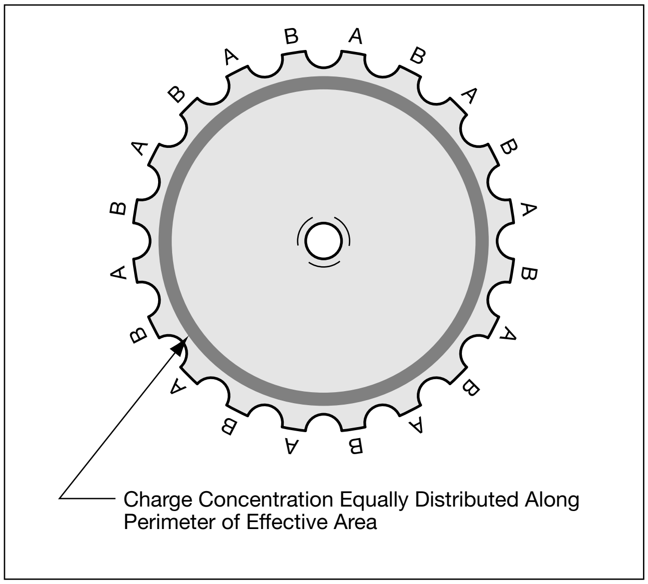


Figure 23. Interdigitated leads.

Plan Ahead

All of the devices mentioned cannot be inserted into an existing layout. Some require special termination pads while others may require a window in the PCB that's already being used. Be aware of the limitations of the different technologies and make allowances for new methods.

Also be careful in that many of these devices are large ceramics. This requires an understanding of the relief necessary when mounting to substrates of different coefficients of thermal expansion. Failure to compensate for a mismatch with these large parts could lead to time dependent failures.



Charge Concentration Equally Distributed Along Perimeter of Effective Area

Figure 24. Circular capacitor with interdigitated leads.

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